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SEPTEMBER 1988

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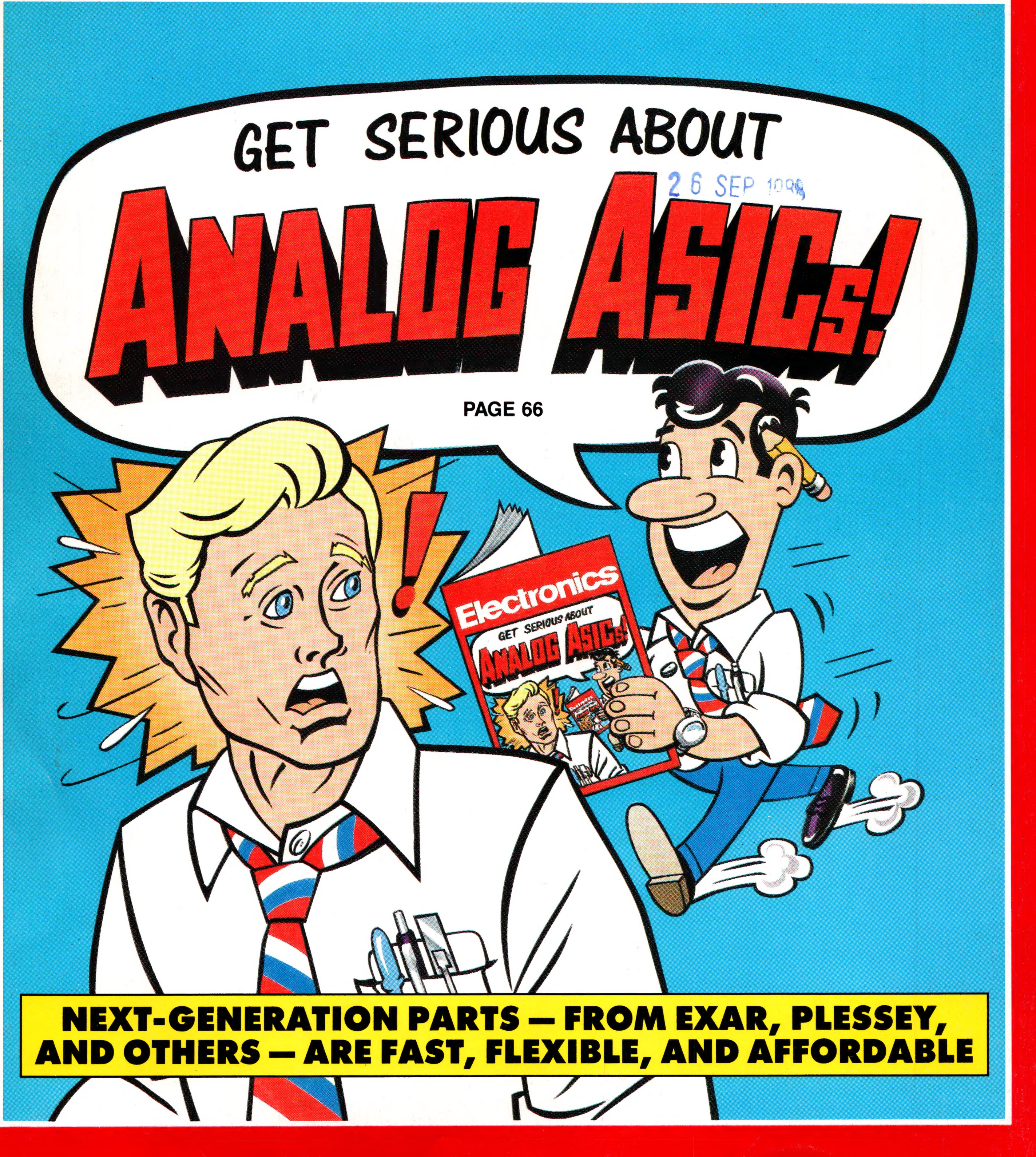

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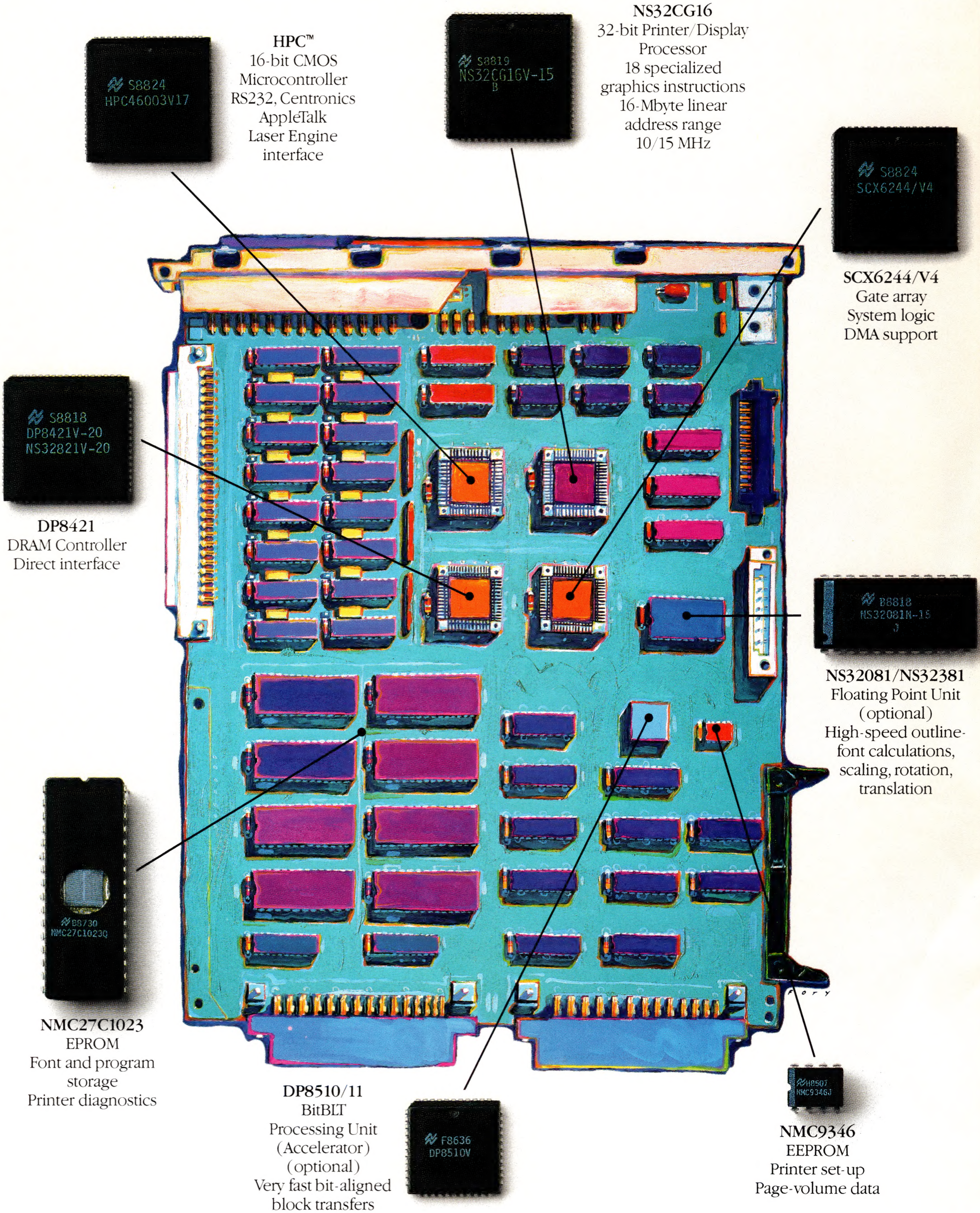

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RS232, Centronics
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interface

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graphics instructions
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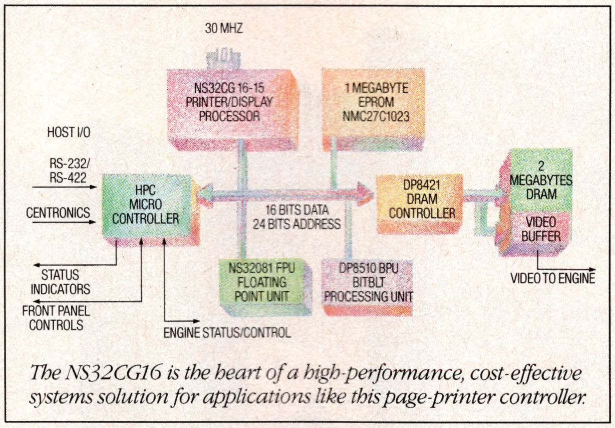
- supports CCITT Group III and IV protocols for facsimile transmission
- on-chip clock generator



The NS32CG16 is the heart of a high-performance, cost-effective systems solution for applications like this page-printer controller.

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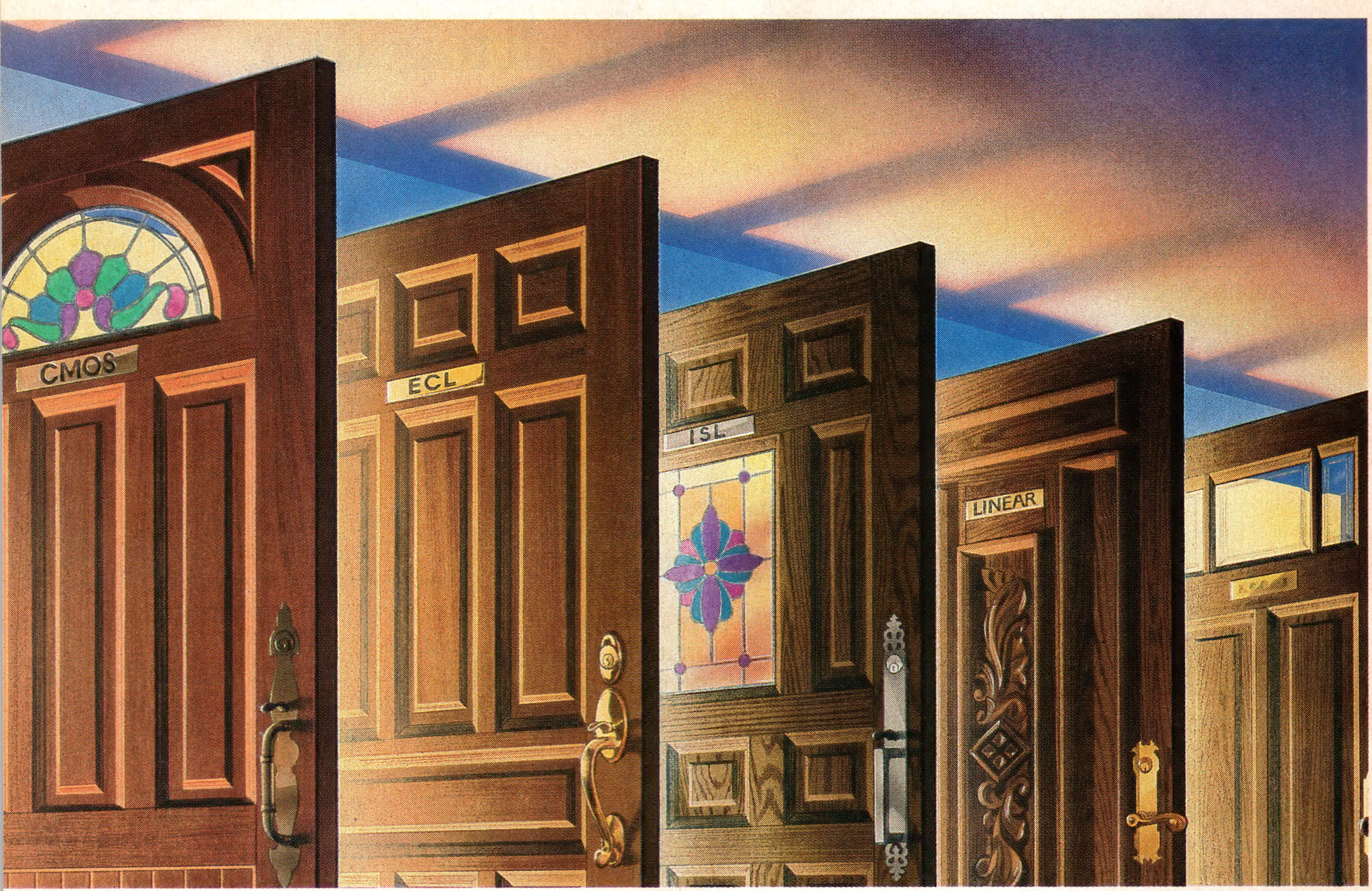

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CAN CHIP AND SYSTEM GROUPS BE FRIENDS?

Not completely, but let's hope the latest strife between an AEA rebel group and the SIA doesn't derail efforts to modify the U. S.-Japan chip accord

Peter makes semiconductors. Paul does systems. Peter is accused of robbing Paul with the aid of the U. S.-Japan chip-trading accord that sets prices on incoming memories and, to some, remains a prime suspect in the 1988 DRAM shortage.

The charges come from a cantankerous band of chip buyers—known in industry circles as the "dissident user group" of the American Electronics Association. The dissidents are now under fire for riding roughshod over frail efforts to unite chip users and producers to support and modify the 1986 U.S.-Japan semiconductor trade agreement.

East and West have met, but will chips and systems factions ever completely agree? Doubtful.

On the eve of the pact's second anniversary this month the chip-using desperadoes unleashed a six-item document. It calls for a complete review of the five-year agreement, and aging U. S. antidumping laws, and seeks an alternative to the foreign-market-value (FMV) system that sets pricing floors on Japanese DRAMs. The group also wants Japan to change the way it deals with dumping in third-world countries, greater access to Japanese markets by U. S. equipment firms, and system-producer representation on the proposed National Advisory Committee on Semiconductors.

Backed into a corner by the influential group, the AEA executive committee has passed the proposal on—minus an even more controversial background paper—to its trade-pact-dealing partner, the Semiconductor Industry Association. Knowledgeable sources close to the SIA say relationships between the two industry groups are being strained by the six-point proposal, and some worry their cooperative efforts could be in peril. Particularly disturbing, says one source, was the leak of the six-point document to an influential newsletter in Washington, D. C. The August leak occurred within days after a joint SIA-AEA proposal won limited concessions from the Commerce Department in FMV setting. The agency had expressed a desire to continue a dialogue because of the SIA and AEA cooperation.

The latest flap is untimely because the AEA and SIA are set this month to launch four new task forces to hash out burning U. S.-Japan issues (market access, extraordinary measures, antidumping, and long-term policies). Let's hope they'll still be talking at the trade pact's third anniversary.

J. ROBERT LINEBACK

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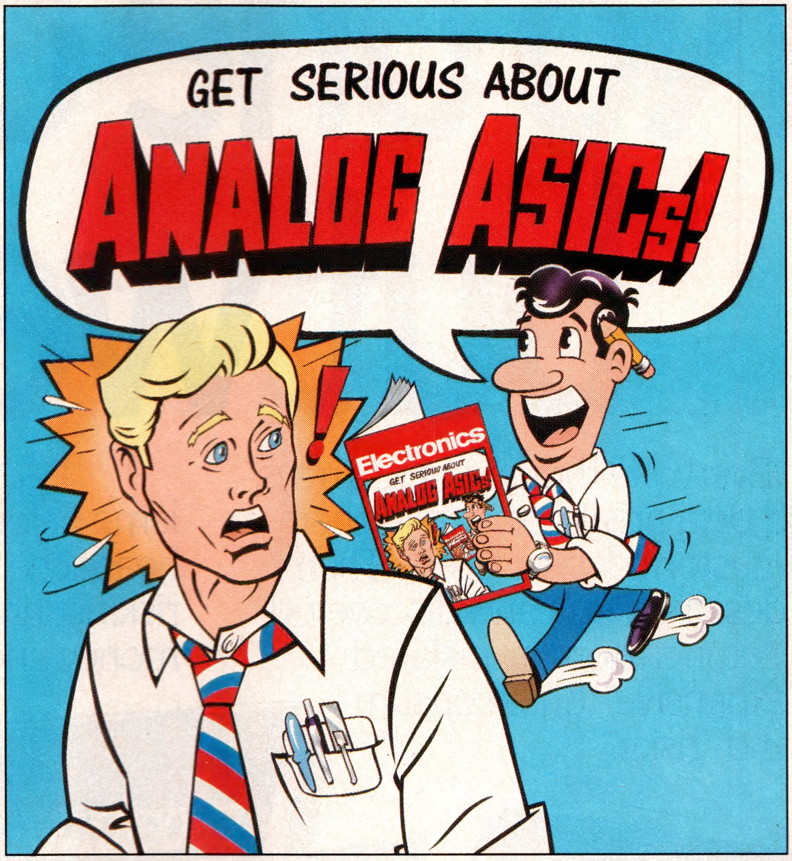
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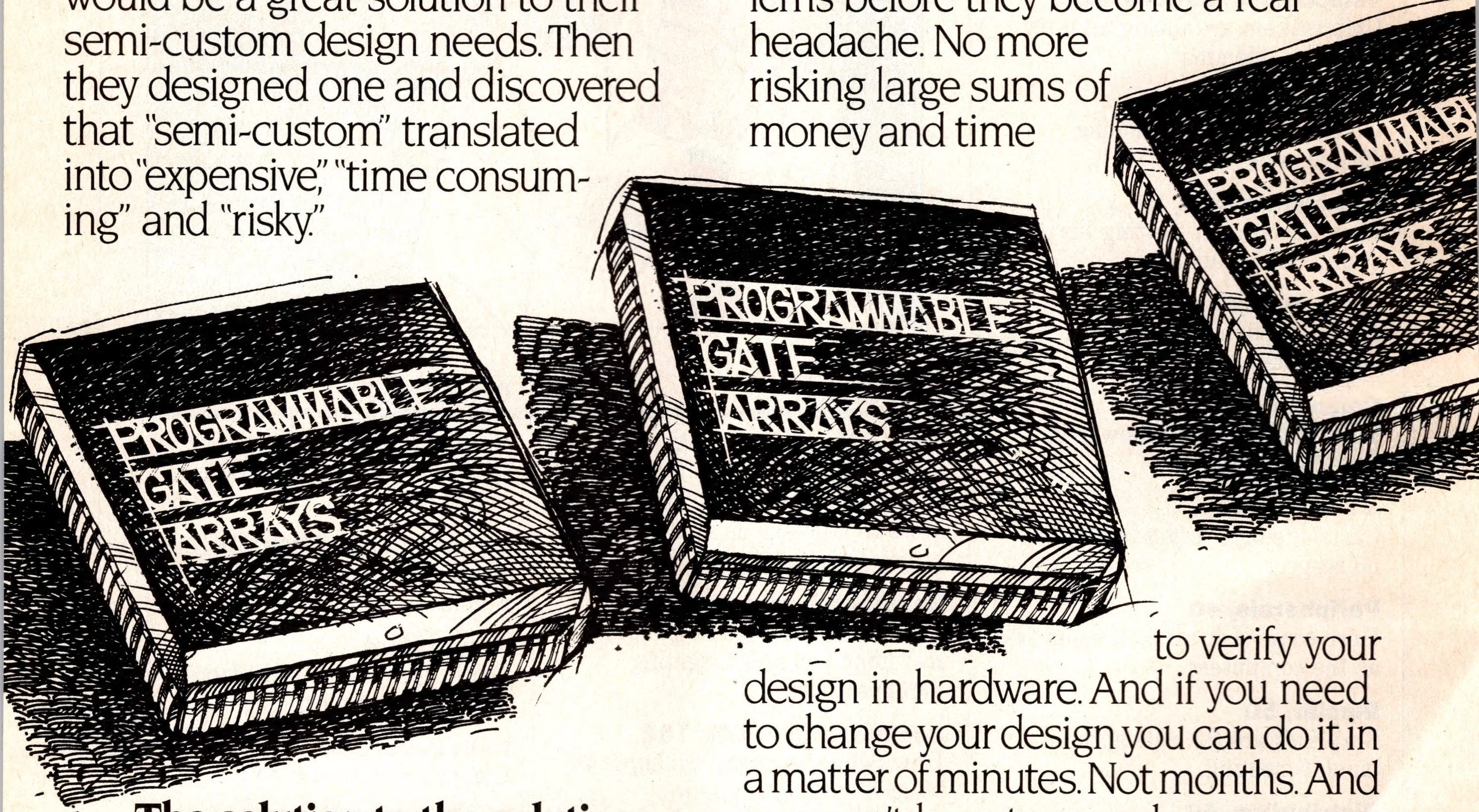
No one can sol but we solve

Everyone thought gate arrays would be a great solution to their semi-custom design needs. Then they designed one and discovered that "semi-custom" translated into "expensive," "time consuming" and "risky."



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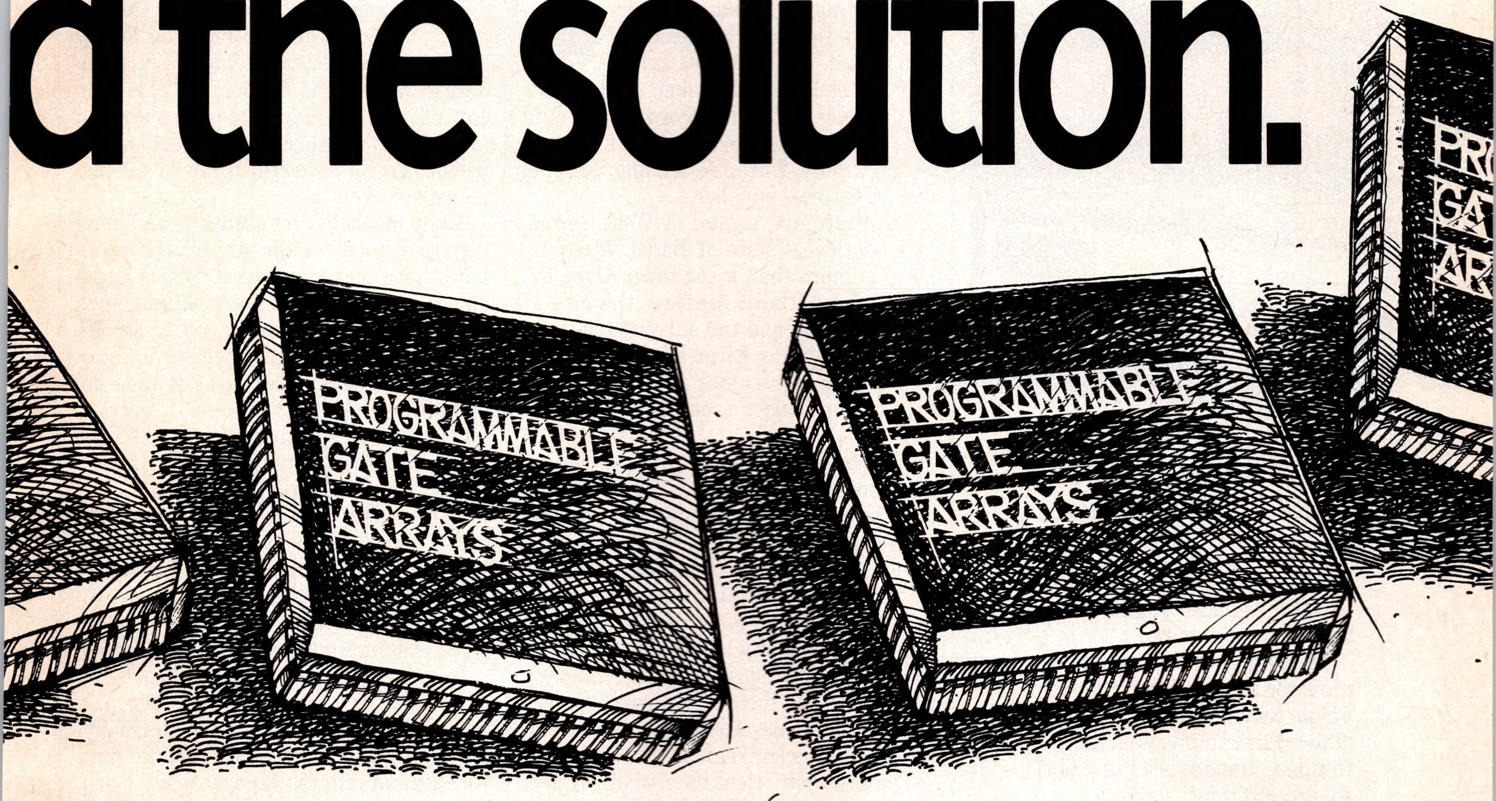

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LETTER FROM STUTTGART

HOME OF MERCEDES NOW RIVALS MUNICH AS TECH HUB

STUTTGART, WEST GERMANY

The city's prime industry doesn't match the volume of Detroit's, but mention Stuttgart and what comes to the minds of many Germans is their country's foremost car production center. The city is the home of Daimler-Benz AG, maker of Mercedes automobiles, as well as Porsche AG. And it is also the headquarters of Robert Bosch GmbH, Europe's leading automotive accessories supplier.

But Stuttgart, capital of West Germany's southwest state of Baden-Wurttemberg, is more than a car town. Over the years and without fanfare, the city of 565,000 people and the surrounding area along the Neckar River have become an impressive electronics region, rivaling the greater Munich area 120 miles to the east.

This so-called Middle Neckar region has about 200 electronics firms in a 30-mile radius around Stuttgart. Besides being a booming production center, it is also a showcase of research and development. In all, Baden-Wurttemberg has more than 40 industry, government, semiprivate, and university labs and institutes as well as a healthy sprinkling of technology parks, many of them active in electronics and related fields. About one-third are in the Middle-Neckar region.

The research orientation is an old one: the predecessors of Standard Elektrik Lorenz AG (SEL) in Zuffenhausen invented the coin-operated telephone in 1891 and radio-beam navigation in 1907. And the tradition is a rich one: out of the labs of IBM Corp. in Böblingen came merged-transistor logic in the early 1970s, and from the Max Planck Institute for Solid State Research in Büsnau came Klaus von Klitzing, winner of the 1985 Nobel Prize for Physics, for his discovery of the quantum Hall effect.

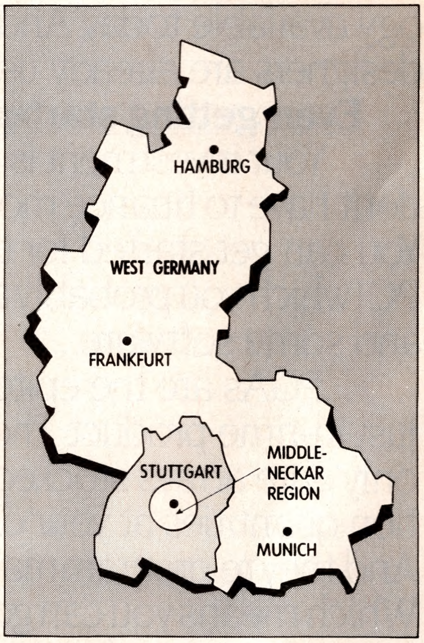
STRONG PRESENCE. The strong presence of R&D in Baden-Wurttemberg stems from the state's farsighted economics policy. After World War II, when many of West Germany's 11 states were less than eager to welcome research institutes, Baden-Wurttemberg embraced them wholeheartedly, recognizing their potential to stimulate economic and technological growth.

And so they did. Last year the region produced $7 billion worth of electronics, and industrially, what once was Europe's poorhouse is now West Germany's richest state. At $18,746, the per-capita gross national product is the country's highest. "It's these [research-oriented] institutes that have acted as crystallization points for small firms and helped turn the Middle Neckar region into a high-tech area," says Walter Löckle, deputy director of the Policy Department in Baden-Wurttemberg's Ministry of Economics. This is in contrast to the electronics belt around Munich, where the catalyst function was performed by powerful Siemens AG and aerospace firms.

Many institutes get state aid, and in return they must engage in applications-oriented research and make results available to local industry. Exemplifying such cross-fertilization is the Institute for Microelectronics Stuttgart, whose director, Bernd Höfflinger, pioneered the ion-implanted n-well CMOS process [*Electronics,* Jan. 22, 1987, p. 16]. IMS circuits have sharpened the competitive edge of local firms' products on global markets.

"The interplay of institutionalized R&D, contract research, and technology transfer as encouraged and supported by the local government is exemplary," Höfflinger says. "That makes this region an ideal location for the industry."

Indeed, in a recent nationwide poll, top managers rated Stuttgart as the preferred industrial site in West Germany, ahead of Munich and Frankfurt. So have foreign managers. Japan's Sony Corp. has moved the headquarters for its European TV operations to Stuttgart, from Wales in the UK, because company exec-



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utives ranked the city and its surroundings as Europe's best high-tech center.

The backbone of the region's electronics industry is made up of giants like IBM, a fixture since the 1930s and now employing 12,000 people, and SEL, which moved from Berlin after the war and has a payroll of 8,500. Then there's Bosch, which is fast turning from a car-parts maker into an electronics producer. Founded in 1886, it employs 40,000 in the area.

But the region's sinews are its small- and medium-size firms, often more dynamic than the big ones. The small-shop industry has a long tradition in Baden-Wurttemberg. "With no mineral resources, no steel, no shipbuilding, and little farming, Germany's southwest was once Europe's poorhouse," Löckle says. So to survive, people who didn't emigrate had to engage in handicraft. That has led to a brand of workers the Germans call "Tüftler": people doggedly determined to solve mechanical problems and invent things.

The Tüftler have spawned the clock industry in the Black Forest (symbolized by the cuckoo clock), the small metal-processing shops that dot the state, and eventually the backyard machine-building industry. In such a small-shop environment Gottlieb Daimler, in 1886, built a gasoline engine that was light enough to power a car.

Today, more than 95% of Baden-Wurttemberg firms employ less than 500 people. "The Tüftler mentality lives on in electronics," says Wolfgang Wolf, head of the Baden-Wurttemberg chapter of West Germany's Electrotechnical and Electronics Industry Association.

In the Middle Neckar region, the number of small high-tech firms has risen steadily over the years. "The increase has been particularly strong for office-equipment and data-processing firms," notes Ulrich Lehmann, chief of the communications section in the Economics Ministry. From 1982 to 1988, their number has shot up 22% and their employment increased 49%, he says. During that six-year period, the new companies have raised their output and exports a whopping 200% and 190%, respectively.

Also doing well are firms engaged in software and the so-called C-technologies (CAD, CAM, and CAQ, for computer-aided design, manufacturing, and quality control). The recent spate of startups in these fields has made the region West Germany's center of activity in C-technologies, Lehman says.

And the fact that the small firms are flourishing seems to be drawing the interest of some large ones, too: Nixdorf Computer AG, for example, plans to set up a computer-integrated manufacturing center in the Stuttgart region employing 2,500 people. Also, machine-tool builders thrive because the electronics technology needed to make their products competitive on world markets is readily available.

Besides the infrastructure of research institutes, another factor making the Middle Neckar region alluring is what Wolf calls "the state's industry-friendly policy." The budget for helping small firms get started is about $215 million a year. This money comes in the form of funds for development programs, low-interest loans, or other incentives. "The business climate here is good," concurs Martin Oppold, sales director at the Novotechnik KG, a manufacturer of precision potentiometers employing 290 people in Ostfildern. One factor, he says, is the state's efforts to promote exports. "Also in our favor is the proximity of big customers like Bosch and the car industry."

From cuckoo clocks to Mercedes to a Nobel in physics

Beyond that, the presence of top-notch educational facilities also adds luster—among them are the Universities of Technology in Stuttgart and Karlsruhe, the engineering school in Esslingen, and a multitude of trade schools. "This infrastructure is important, since it makes available the kind of engineers and technicians that institutes and the industry need," says Höfflinger.

No less an asset are the people. Swabians, as the inhabitants of southwest Germany are called, have a reputation for being well-trained and taking work seriously. A well-known Swabian saying, in their dialect, is "Schaffe, schaffe, Häusle baue," meaning roughly, "Work, work, to build a small house"—a motto that also points up their pride in ownership.

And the pride seems to extend to their jobs. "Given the concentration of high-tech firms, there's some job-hopping in the Middle Neckar region," says Engelbert Totsche, a manager at SEL. "But a fairly strong loyalty keeps the fluctuation below the country's average." People are also loyal to Baden-Wurttemberg. "I, for one, would not want to move to northern Germany," Totsche says.

No wonder. With its rolling hills, beautiful Lake Constance, the Black Forest, and excellent cuisine, Baden-Wurttemberg is among Germany's more desirable places to live. And Stuttgart itself, where the vineyards stretch almost to Daimler's engine-production plant, has much to offer in the way of culture—ballet, theater, museums. It is no longer the provincial town that it was only twenty years ago.

Overall, Baden-Wurttemberg accounts for 1.7% of the world's trade volume, which is more than all of Sweden, Switzerland, or even Brazil. And the Stuttgart area's electronics industry has been a major contributor to that wealth. *–John Gosch*

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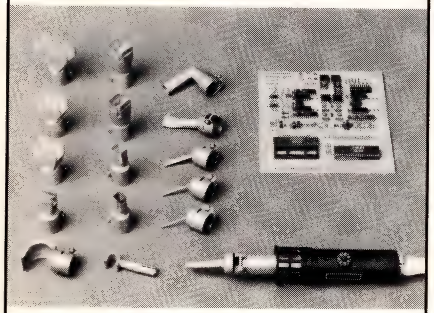

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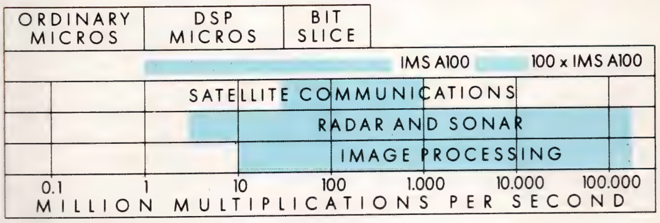

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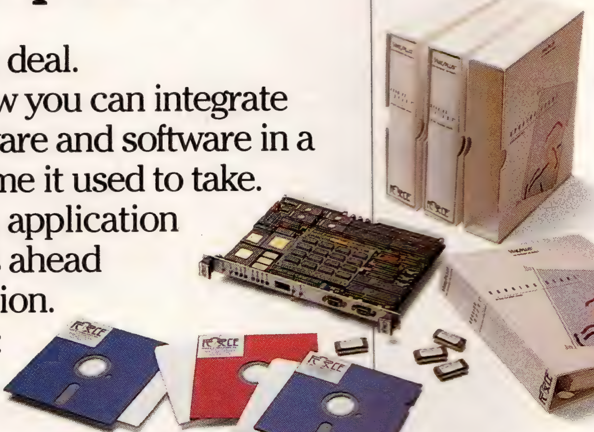

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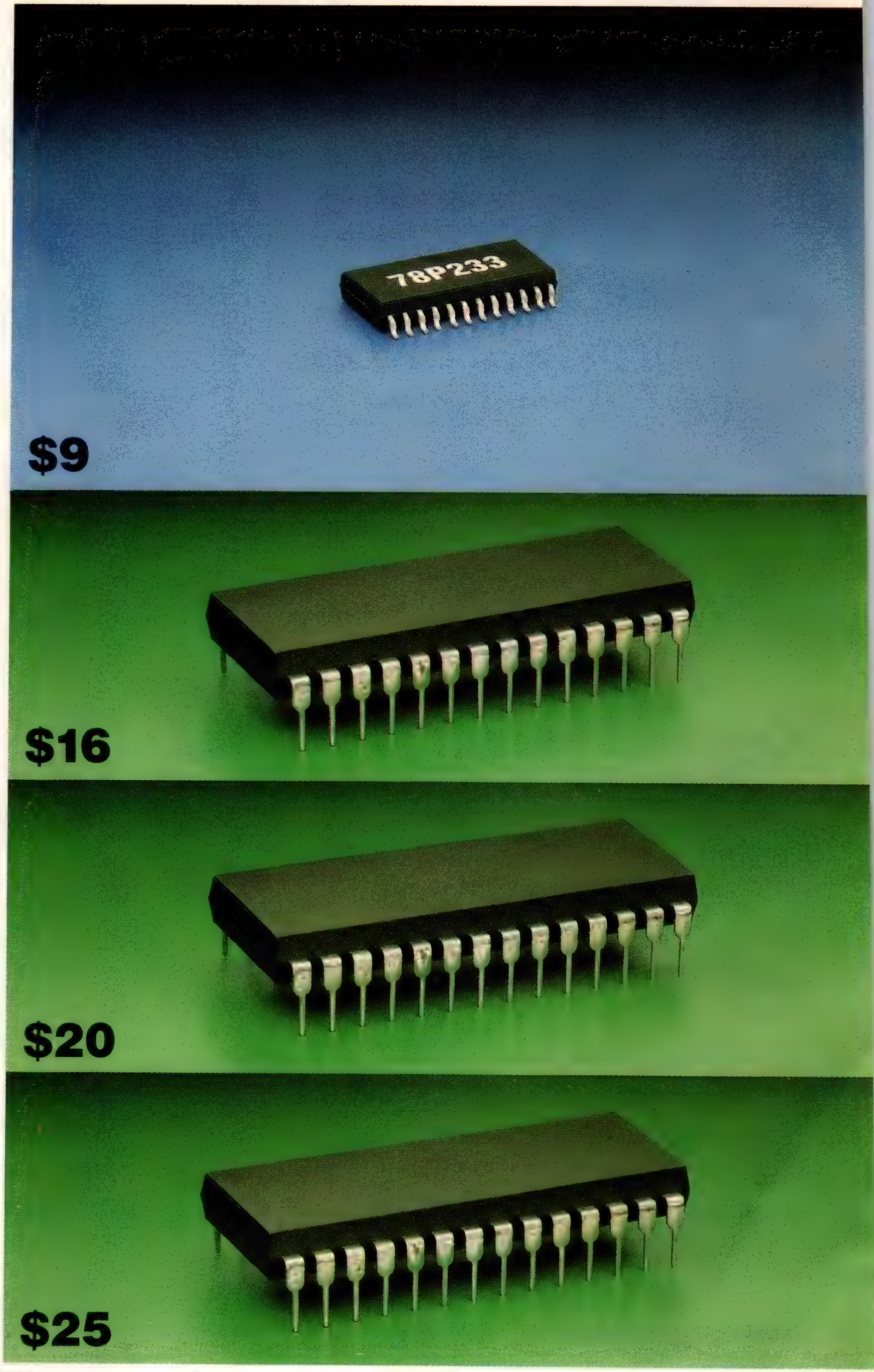

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ELECTRONICS NEWSLETTER

U. S. CHIP MAKERS' SHARE IN JAPAN STILL ISN'T GROWING FAST ENOUGH

U. S. chip merchants are gaining market share in Japan at only one third the rate needed to hit the 20% target set in the 1986 U. S.-Japan semiconductor accord. The Semiconductor Industry Association's second annual report on the accord, which is due out this month, concludes that U. S. chip makers had a little over 10% of the market in Japan by the end of June, only slightly higher than the 8.5% share they had two years ago. At that rate U.S. firms will have only a 14% share by 1991, when the 20% target is supposed to be met, the SIA says. Moreover, the gain in this year's second quarter was just 0.2% instead of the expected 0.6%. Don't blame Japan's giant electronics conglomerates, though. SIA figures indicate that Japan's top five electronics companies are buying about 17% of their chips from U.S. sources—nearly three times that of the country's smaller systems houses. ☐

HEWLETT-PACKARD POURS ON THE STEAM IN THE IC TESTING MARKET . . .

A shakeup is rocking the market for integrated-circuit test equipment—and Hewlett-Packard Co. is trying to benefit. Former industry leader LTX Corp., Westford, Mass., has lost ground and fallen behind Advantest, says G. Dan Hutcheson of VLSI Research Inc. in San Jose, Calif. LTX's linear tester sales have fallen 31% since 1985, he says, from a high of $111 million to around $71 million, mostly because the company hasn't been able to field a competitive upgrade to its MTS77 tester and because of problems with product reliability, he says. Meanwhile, HP has taken the market by storm. HP's first offering was the HP9480, introduced in December 1986, and the Palo Alto, Calif., company has since garnered a 7% share of the world market. LTX's Hi.T tester, however, has won only a 2% share. With two major system sales in August—worth a combined $1.8 million—HP appears to be pouring on the steam, putting the pressure on LTX, which is struggling to complete development of its long-awaited Synchromaster machine. ☐

. . . AND IT GOES INTO THE THIRD-PARTY SUPPORT BUSINESS

Can an electronics giant parlay its reputation for top-notch service and support into a lucrative new business? Giant Hewlett-Packard Co. thinks so. It set up a separate operation to pursue maintenance contracts with Fortune 1,000 companies for what it terms office work stations—everything from desktop computers to networks—of all manufacturers. The potential payoff is an eye-opener: HP says the third-party support market totaled $2 billion in 1988, and will grow to $3.5 billion by 1990. Everyone from local retailers to General Electric and Xerox handle the work now. But HP figures the time is ripe for a major effort because "people now look at service as just another product they buy," says David M. Carver, operations manager of HP's new Multivendor Support Operation. ☐

OPEN SOFTWARE FOUNDATION WILL BE AT HOME IN CAMBRIDGE

The Open Software Foundation is doing its bit to make Cambridge, Mass., more of an international software hub [*Electronics*, August 1988, p. 8]. OSF rejected locations in Pittsburgh, Pa., Austin, Texas, and Washington, D.C., to locate its expected 200-person staff in a building Symbolics Inc., the struggling artificial intelligence vendor, once occupied. The consortium was formed this spring to challenge what its original eight members charged was an AT&T and Sun Microsystems Inc. conspiracy to control the evolving Unix operating system standard. Now boasting 25 members, an office in Brussels, Belgium, and seeking a Japanese site, OSF is developing some open software standards beyond Unix, including user interfaces and data base systems. ☐

ELECTRONICS NEWSLETTER

DEC FIRES UP AN ENTERPRISE-WIDE NETWORKING STRATEGY

Digital Equipment Corp. is turning up the fires on IBM Corp. with a huge array of software and hardware products that facilitate and speed enterprise-wide networking—communications between local- and wide-area networks comprised of DEC and IBM systems. The cornerstones of the new line are the MicroServer, which is a modified MicroVax II communications server that's four times faster than DEC's current Ethernet solution; and a wide-area synchronous interface that provides MicroVax systems with 64-Kbit/s and 256-Kbit/s wide-area communication links. But DEC is pushing IBM's buttons with software. DEC has developed a pair of DECnet-to-SNA gateway packages that let DECnet users exchange data between IBM Systems Network Architecture computers and DEC machines produced with similar equipment.□

TI's NUBUS INTERFACE CHIPS COULD MAKE LIFE EASIER FOR APPLE

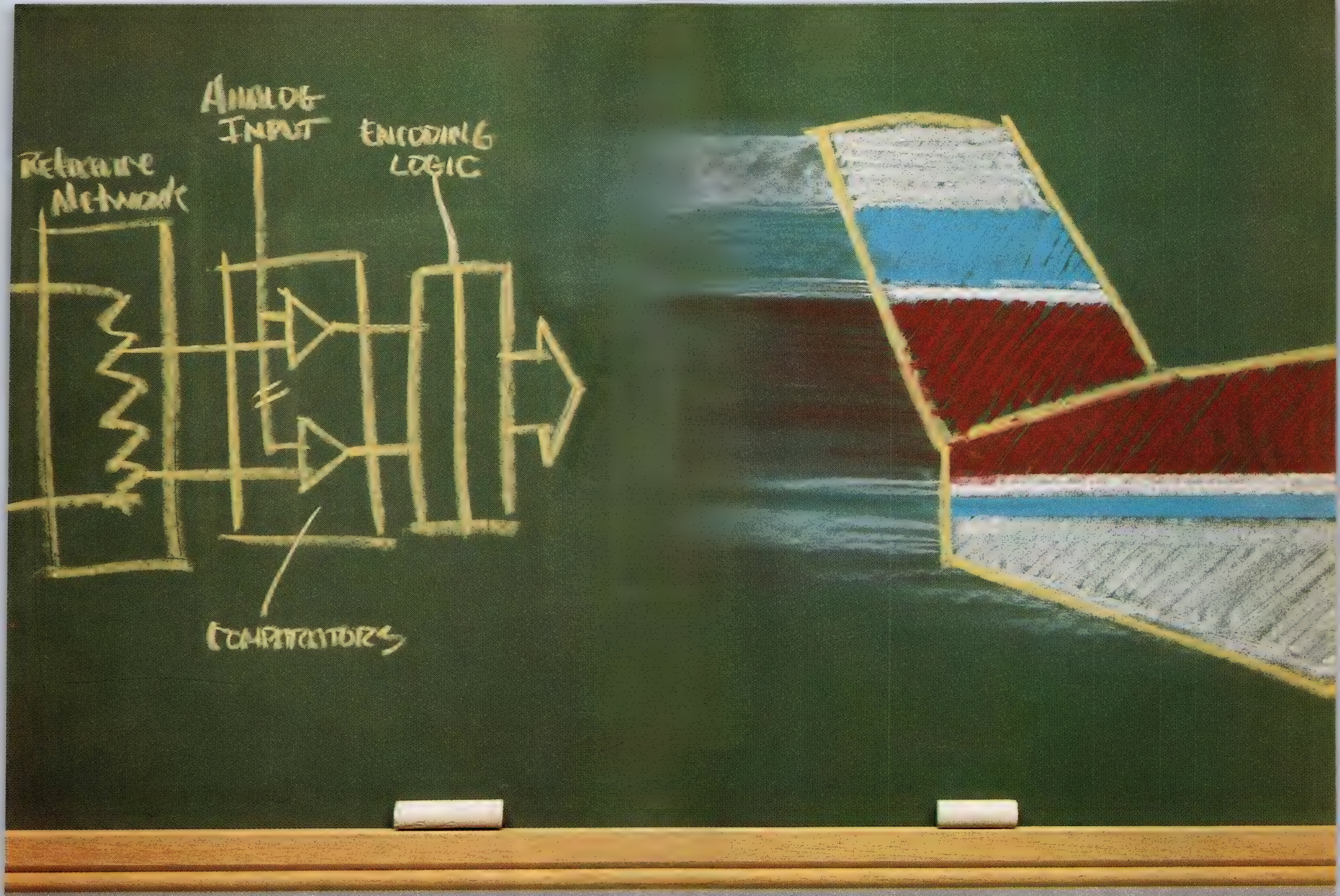
Strengthening the NuBus as a contender among 32-bit computer backplane standards, Texas Instruments Inc. is bringing to market the industry's first standard family of NuBus interface chips this month. The chips were designed with the aid of Apple Computer Inc.—the only major systems house to embrace NuBus so far when it chose the multitasking scheme for its Macintosh II Open System. The new chips, which include a 32-bit interface controller and a 16-bit address/data transceiver chip, will help make it easier for Apple to develop a more efficient next-generation Mac, because the two eliminate the need for as many as 45 logic chips. What's next? TI and Apple are working together to develop a separate 1-μm CMOS chip that integrates most of the NuBus master interface logic of the Macintosh Coprocessor Platform. Although primarily used today for add-in boards for the Mac II, TI says NuBus could be used in engineering work stations and in personal computers based on Intel Corp.'s 80386 microprocessor. □

TOSHIBA AND TRON ENTER THE EMBEDDED CONTROLLER MARKET

Japanese chip makers have steered clear of embedded-control chips over the years, leaving the niche to such U. S. powerhouses as Intel Corp. and Motorola Inc. But now Toshiba Corp. is trying to turn things around with the TX-1—the first 32-bit embedded-controller chip ever to come out of Japan. Aimed at high-speed embedded-control applications, the TX-1 will go head to head with Intel Corp.'s 80960, a reduced-instruction-set-computer chip aimed at the same market. Both parts will debut late this year. The TX-1 is also the first application of TRON—The Real-time Operating Nucleus—in embedded control. The chip, which integrates 450,000 transistors on a 10.89-mm by 10.27-mm piece of silicon, has an average operating speed of 5 million instructions/s and can peak out at a swift 12.5 mips. □

HUGHES FINDS A USE FOR GERMANIUM IN SPACE-BASED SIGNAL PROCESSING

There may yet be an important place in technology for germanium, the material that ushered in the transistor age but was replaced by silicon. GMHE/Hughes Aircraft Co. says research it's doing for the Strategic Defense Initiative shows that a new germanium chip is better at processing data gathered by infrared sensors than a silicon alternative. The entirely germanium chip includes the world's first FETs built from germanium junctions, say officials at Hughes' Electro-Optical and Data Systems Group in El Segundo, Calif. Hughes says the germanium-readout technology is more tolerant to radiation from nuclear detonations in space and needs less power than silicon. It's intended for use with large, infrared focal-plane arrays SDI would use to track in-flight ballistic missiles while they are outside the earth's atmosphere.□



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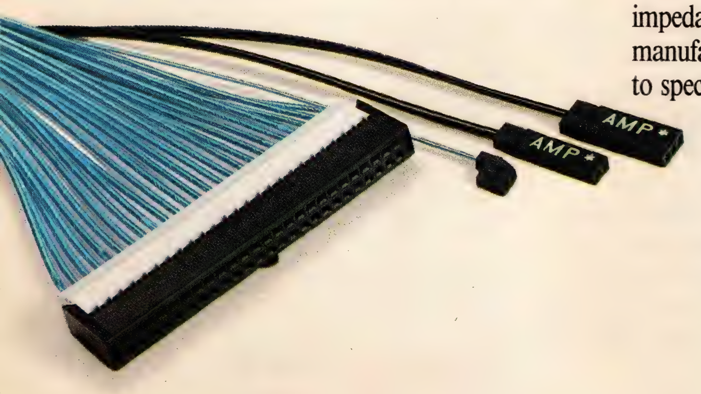

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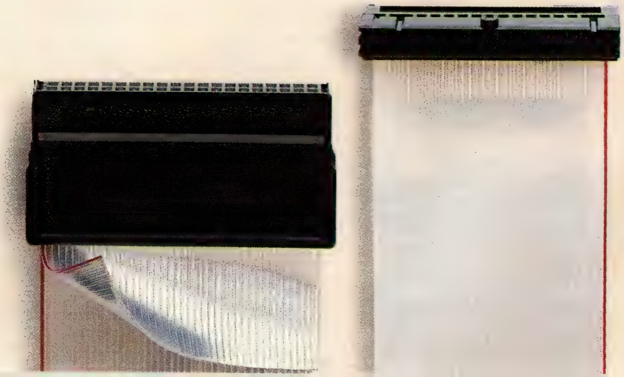

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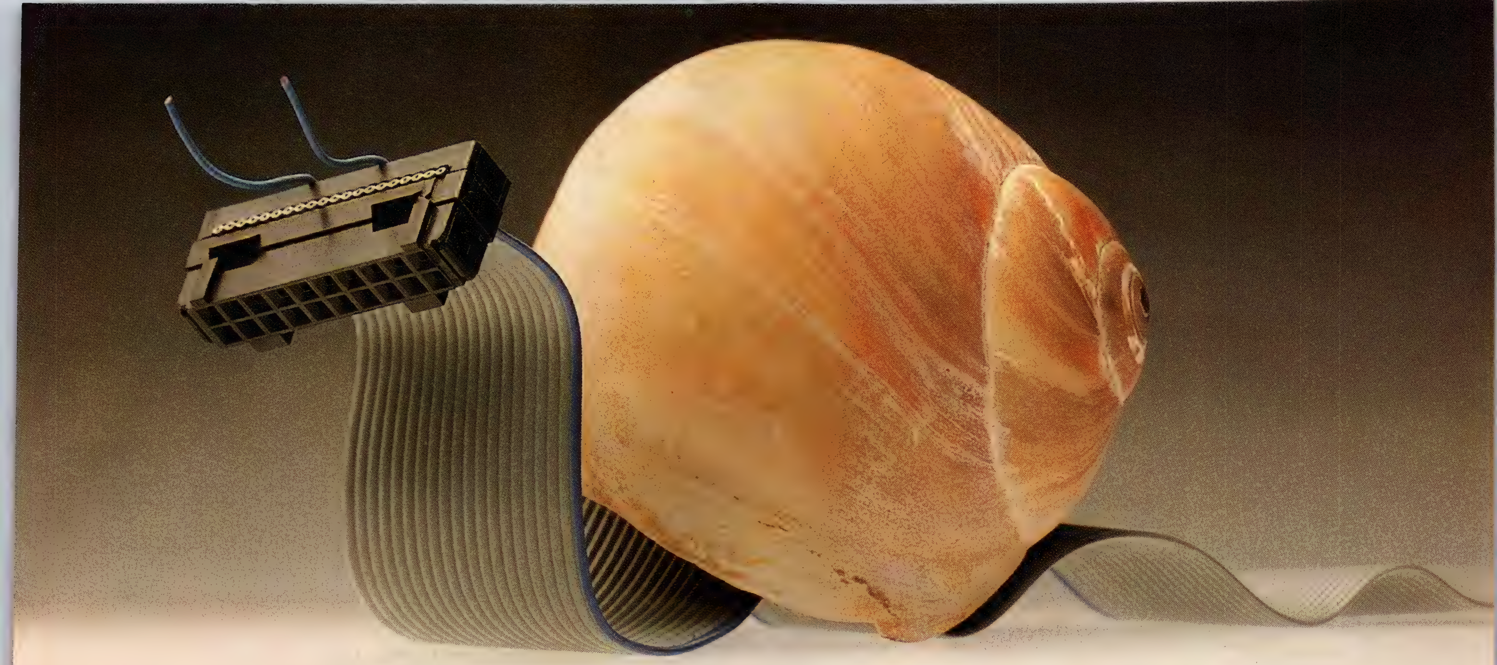

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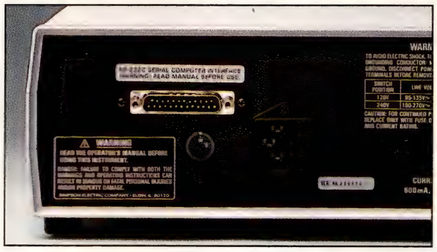

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PRODUCTS NEWSLETTER

FUJITSU'S ECL LOGIC BOASTS 3-GHz CLOCK SPEEDS

A trio of ECL logic families from Fujitsu Microelectronics Inc., San Jose, Calif., offers choices optimized for speed, power, or pin compatibility. The speed-demon MB880 series operates at clock rates of 3 GHz, but each logic function (gate, flip-flop, multiplexer, demultiplexer, etc.) consumes 250 to 1,200 mW and costs about $120 per chip in 1,000-unit quantities. The power-optimized MB810 series offers functions similar to the 880 series but runs at 1.5-GHz peak clock frequency and dissipates from 50 to 150 mW. It costs about $15 per chip. The 10KHL series, as its family name implies, drops into sockets already established for Motorola's 10KH ECL logic family. But Fujitsu's process cuts the power dissipation to half that of the 10KH series—to just 13 mW/gate. Prices for the 10KHL chips will be slightly higher than their 10KH predecessors. All the logic families will be available soon. ☐

SYMBOLICS' IVORY CHIP MAKES ITS DEBUT—IN A MACINTOSH II

The long-awaited Ivory 32-bit symbolic/Lisp microprocessor from Symbolics Inc. has hit the street running. It's in an Apple Computer Inc. Macintosh II host called MacIvory. The artificial-intelligence work station aims to give Texas Instrument Inc.'s MicroExplorer—another Mac II product—serious competition at the low end of AI. A value-added-reseller agreement with Apple, Cupertino, Calif., makes Symbolics the exclusive MacIvory source. A standard system includes the Mac II, Ivory add-in board, NuBus interface, and Symbolics Genera software. Prices for the MacIvory start at $21,900, with deliveries set for December. Symbolics, Cambridge, Mass., says MacIvory will appeal to developers because of Genera's richness and the simple procedure calls that let users invoke either the host Mac or Ivory processor. ☐

GaAs LINE DELAY HYBRIDS ARE FIRST FRUITS OF $30 MILLION PENTAGON PROGRAM

Acoustic-charge transport technology—heralded as the missing link between the Pentagon's Mimic and VHSIC programs [*Electronics,* July 1988, p. 29]—is making its commercial debut in two versions of a selectable line delay offered by Electronics Decisions Inc., Urbana, Ill. Based on gallium-arsenide technology and a result of the Pentagon's $30 million ACT program, both standard parts are programmable by an 8-bit digital control word. The SDL06CBAA handles 150-MHz bandwidths and gives 64 selectable delay settings at 11.2-ns increments. The SDLO7BAAA provides 128 delay settings at 5.6-ns intervals at up to 50 MHz. Housed in a 2.6-by-1.6-by-0.3-in. package, the devices' compactness will pay dividends in jobs including electronic warfare and medical instrumentation by replacing multiple components. The standard SDL parts will sell for about $5,000 for single units, but are projected to drop to below $1,000 for quantity within a year. ☐

TEK SCOPE COMBINES THE BEST FEATURES OF SCOPES, ATE FOR ASIC TESTING

Users of application-specific integrated circuits and complex circuit boards made with ASICs can now get the high-pin-count capability of automated test equipment and the flexibility of oscilloscopes in a new digital sampling oscilloscope from Tektronix Inc. The Beaverton, Ore., company's 11801 uses a multichannel expander plug-in module to acquire and measure up to 136 channels simultaneously at 1-ps timing resolution. It handles all channels at frequencies up to 20 GHz—fast enough to test ECL and GaAs circuits. Another plug-in board delivers differential time-domain reflectometry measurement capability for measuring impedance and propagation characteristics of transmission lines and networks. Price for the 11801 mainframe is $23,500; the multichannel expander, $10,000; and a TDR head, $5,000. ☐

PRODUCTS NEWSLETTER

NEC STARTS ITS DRIVE FOR A TWO-CHIP 2,400-BIT/S MODEM

NEC Corp. is joining the race toward minimal chip counts for modems with an integrated circuit that handles all the digital functions for full-duplex 2,400-bit/s modems and half-duplex 4,800- and 9,600-bit/s devices. What's more, a second chip implementing all analog modem functions is on the way from the company in Kawasaki, Japan, which means a modem could be built with two VLSI devices. To maintain compatibility with existing software, the μPD77810 includes a 16-bit digital signal processor compatible with NEC's μPD77C25 and an 8-bit one-chip controller compatible with NEC's μCOM78K/I. Fabricated in 1.2-μm CMOS, the μPD77810 can also be used for other applications, such as speech synthesis, that require a digital signal processor and controller. Working with other chips, it can handle full-duplex modems for 9,600 bits/s and higher speeds. NEC will start taking orders for ROM codes for the device in December. In lots of 10,000, the chip is priced at about $50 each. Production will begin in April. ☐

BOARD SET WEDS IBM PC COMPATIBILITY TO VME AND VXI BUSES

VMEbus system builders can build industry-standard IBM Corp. Personal Computer features in their products with Radix Microsystems Inc.'s EPC-1 embedded PC. The Beaverton, Ore., company's two-module set integrates a fully-PC-compatible 386-based computer with a full VMEbus interface. It's the first such computer for VMEbus and also the first machine to provide direct support for the VME Extensions for Instrumentation (VXI), a modular-instrumentation bus standard. The EPC-1 is available with either a 16- or 20-MHz Intel Corp. 80386, up to 4 Mbytes of random-access memory, an EGA graphics controller, and floppy and Small Computer System Interface hard-disk controllers. The SPC-1000 development system, which has windows, software, and a PC-to-EPC program migration link, is available for $7,950. ☐

3M'S TAPE CARTRIDGE SQUEEZES 128 MBYTES INTO PC TAPE DRIVE

The lead in 3½-in.-form-factor tape drives has shifted to 3M Corp.'s MCD-Series II, which records 128 Mbytes on a single DC2000 cartridge. It extends its capacity—most 3½ in. drives store about 40 Mbytes—with an extended length media. The MCD series stores 86 Mbytes with a standard length 205-ft. cartridge. Being sampled this month, the drive uses a modification of the industry standard QIC-100 format, say officials at the 3M Magnetic Media Division in St. Paul, Minn. The jump in capacity comes in time to meet the demand for data-storage backup for IBM Corp. PS/2 computers. The 3M drive uses the Small Computer System Interface common command set, and records 16,000 bits/in. on 32 serpentine tracks. Read-write operations are at 90 in./s, and data-transfer rates of 6 Mbytes/s are more than double 3M's existing QIC-100 drives. Pricing in volume is about $480 each. ☐

OUT OF THE LAB, INTO THE FIELD WITH FLUKE'S TRAVELING CALIBRATOR

John Fluke Manufacturing Co.'s 5700A multifunction calibrator boasts such superior temperature stability that it is the first of its type that can be moved out of the calibration laboratory and into the field without losing accuracy. The Everett, Wash., company's $19,950 calibrator is also so easy to use that a technician without a great deal of experience can calibrate multimeters. At frequencies from 10 Hz to 1 MHz, the 5700A provides dc voltage from 220 μV to 1,100 V, and ac voltage from 200 μV to 1,100 V. It also offers up to 2.2 A of dc and ac current with frequencies for ac current ranging from 10 Hz to 10 KHz. A wideband voltage option 5700A-03 provides ac voltage output from 10 Hz to 30 MHz to calibrate rf voltmeters. ☐

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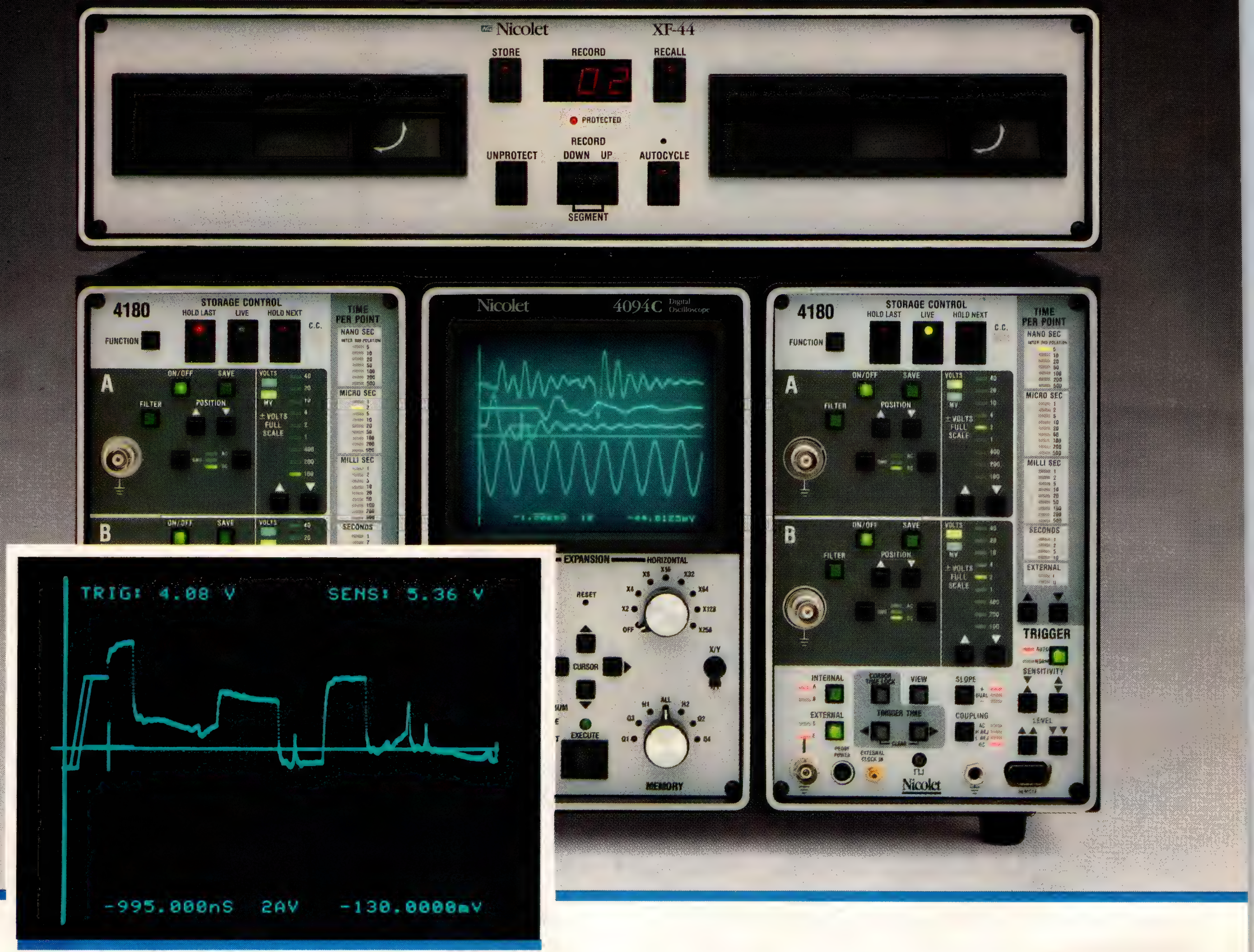

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Electronics

THE PENTAGON IS HOT ON THE TRAIL OF A BETTER WAY TO DESIGN AVIONICS

It would spring from gate-level simulation of chips from different vendors

DAYTON, OHIO

Fundamental changes are in the wind for the way military avionics chips and systems are specified and designed. The Air Force is preparing to launch a program this month in multivendor system simulation that could dramatically slash the cost and time required to develop complex, interchangeable military aviation electronics.

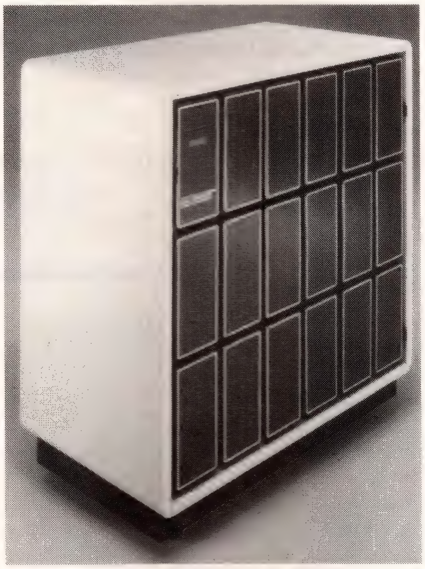
If the Dames program (for Demonstration of Avionics Module Exchangeability via Simulation) is successful, it would be adopted by all U. S. military services, Air Force officials say. And the program could usher in a new era that will require heretofore unthinkable levels of cooperation among archrival competitors in the defense electronics business.

Barring unforeseen glitches, the Dames contract is expected to be awarded in time to beat the Sept. 30 deadline for federal fiscal-year 1988 funding, industry sources say. They peg the value of the two-year Dames effort at several million dollars. The contract is expected to go to Zycad Corp., a St. Paul, Minn., vendor of simulation acceleration engines and software. Zycad would serve as the third-party contractor, simulating gate-level models of different vendors' chips working together. The company has the biggest installed base of simulation equipment as well as the fastest accelerators.

Most defense contractors already rely on simulation at the chip and system levels for internal design verification. But under Dames, military chip vendors for the first time will be required to submit gate-level models of highly proprietary chip designs to an outside contractor.

CATCHING GLITCHES. By catching glitches early—before designs reach silicon—the Air Force is hopeful that gate-level system simulation methodology can reduce the need for multiple iterations of physical prototypes, which must be redesigned because they won't talk to other vendors' equipment. That could save a barrel of time and money. And the technique could also speed development cycles by allowing software engineers to start earlier on microcode development, prior to hardware availability. The idea is to assure true interoperability among chips designed by multiple vendors, in most cases before the designs are fabricated in silicon.

"If I can see a process or a methodology out there that allows me to see things working through integration sooner, that means risk reduction to me. That's how we think about it here," explains Capt. Jack Strauss, manager for avionics architecture and software at the Air Force Advanced Technology Fighter System Program Office at Wright-Patterson Air Force Base near Dayton, Ohio. The ATF office will provide the funding for Dames, but Strauss will say only that the program is "in procurement." And he is quick to point out that the effort is in no way tied to the equipment of any particular vendor.



In the Phase Zero experiment, Zycad used its logic simulator to mesh gate-level designs.

Still, Zycad laid the groundwork for winning the contract earlier this year in an unusual demonstration performed at no charge to the military. In that effort, known as Gate Level System Simulation Experiment Phase Zero, Zycad used gate-level models of chip designs supplied to IBM, Texas Instruments, and Unisys, which also contributed gratis engineering support. The success of that project in ironing out incompatibilities among the three vendors' designs convinced ATF officials to pursue the idea further with Dames.

A major driver for Dames is the need to develop common triservice modular avionics as directed by Congress in the 1987 Defense Appropriations Act. "We've got a requirement for unconditional module exchangeability. What that means is that we've got to have a specification that is absolutely unambiguous, so that anybody can produce this module and I can plug it into my system," Strauss notes. "Those kinds of specifications have never been done before. So we're trying out some things that have never been done before," he says.

BUS STANDARDS. The Dames program will focus on proving interoperability among chips designed to the emerging set of common bus standards born out of the Pentagon's Very High Speed Integrated Circuits program [*Electronics,* April 14, 1988, p. 33]. Even though contractors do their best to adhere to such standards, hardware prototypes of circuits built by different vendors working independently may still not be able to talk to each other, industry officials concede. That's because of ambiguities typical of nascent specifications, which leave some things open to discretion and interpretation by the individual contractors. And that's not to mention pure design flaws that can keep first-pass chips from working properly.

"The thing that gate-level system simulation does for you first, is it helps you understand the interfaces," observes Maj. Robert P. Lyons Jr., chief of the ATF core avionics division. "Secondly, it helps you get the design straight before you ever commit to the high capital costs of developing these chips, and the modules themselves. What became astonishing to us was the notion of having very, very large, VHSIC-class chips going through first-pass success for both fabrication and integration."

Lowell A. Benson, technical director for common module development for Unisys Defense Systems, in Eagan, Minn., says the firm's participation in the earlier Phase Zero effort proved to be worthwhile. "We found a few things within our own design, that if we had not been doing this experiment, we would probably have ended up with silicon that was not completely functional," he says. "As it was, we were able to hold up release for silicon and put in the corrections."

There is also praise for the Phase Zero effort from Sam Estess, integration manager for military computer systems at TI's Defense Systems and Electronics Group in Plano, Texas. "Even before we did the first simulations, just the process we went through could rightly be called a success because we had three competitors together in a room trying to figure out how to talk to each other," Estess says. "We were all very careful about what we told each other, because we didn't want to give away any proprietary data. But there was a lot of good cooperation going around among Unisys, TI, and IBM."

And that kind of cooperation among vendors is a precedent, says Jack Harding, general manager for Zycad's Federal Services Group in Morristown, N. J. "This has never happened before, where industry got together with the military, worked for free, and—by the way—worked with their archrivals to achieve this commonality goal," he says.

The eight-month Phase Zero experiment, wrapped up in August, was performed for the Joint Integrated Avionics Working Group, the triservice organization that was established to ensure that avionics interoperability goals are achieved. In Phase Zero, gate-level models only of Bus Interface Unit circuits were simulated, communicating over the PI-Bus VHSIC backplane bus. And the three participating chip vendors represented defense teams competing on both the Air Force ATF and the Navy's Advanced Tactical Aircraft program.

But Dames will significantly expand on the idea. About a half-dozen chip vendors are expected to take part, including ATF and ATA competitors, as well as contractors working on the Army's Light Helicopter effort. That's important to the joint avionics group, since the goal is true plug-and-play interchangeability not only among modules supplied by different vendors, but also across all three military aircraft platforms.

PAYOFF. Neither industry nor Air Force officials will estimate the potential payoff from Dames. But for his part, Strauss allows that the ability to find and fix flaws during the design stage—as opposed to later fabrication stages—could produce cost savings for the military of "one or two orders of magnitude."

The effort may eventually lead to a new way of developing military specifications, which might rely upon gate-level descriptions in addition to a written specification documents, Strauss says. "The transitioning of what has classically been VLSI design technology into a specification methodology is one thing we're hoping to get as an artifact of Dames," he notes. And that, Strauss says, could represent "a fundamental change in the way we do business." *–Wesley R. Iversen*

TELECOMMUNICATIONS

CHIP MAKERS FACE ISDN SOFTWARE DILEMMA

NEW YORK

Chip makers that a year ago were praising the way their chip sets implemented the emerging protocols, interfaces, and functions of the integrated services digital network have a tougher sale ahead in 1989: building credibility in the complex software that runs their silicon.

Credibility has always loomed large on ISDN's impressionistic landscape, and should continue to be its bugaboo through the end of the decade. In no small part, the "Does it really work?" attitude of prospective customers evolves from the magnitude of the problems inherent in achieving ISDN's lofty goal: Delivering integrated voice, data, videotex, and facsimile to the desktop or kitchen table—and with worldwide connectivity.

Not unexpectedly, the International Telegraph and Telephone Consultative Committee is moving slowly in adopting ISDN standards. But the chip makers, locked in a struggle for a dominant position when the market blooms, can't wait. They are busily stitching together semistandard solutions that for the interim at least will result in islands of ISDN. Much of the action is on the software front, where three factors are at play. Central-office switch makers have each gone their own way in interpreting ISDN's nascent signaling procedures, which requires chip makers to write different software modules for each switch.

IC houses must provide separate software modules for each switch

Further complicating chip makers' lives is an uneasiness about semiconductor houses diving into the unfamiliar waters of telecommunications software. And then there's the issue of conformance testing.

It all begins with the CCITT. Through its Q-series of ISDN recommendations, the CCITT will soon begin focusing on the ISDN's supplementary services. These services, which are governed by Q932 recommendations, include call waiting, call forwarding, automatic caller identification, automatic call back, and the like, says Randy Spusta, district manager for ISDN and data standards at Bell Communications Research Corp., Navesink, N. J.

Most of these services are already being implemented in the present generation of switching equipment, but ISDN will handle them in a fundamentally different way. It requires more intelligence to be built into the customer's equipment, which, among other things, eliminates the interrogatories that now go on between the switch and customer to find out what service is to be invoked. Making all that automatic and universal takes standards.

Bellcore, the research arm of the seven Bell regional operating companies, plays a key role in standards monitoring and development for U. S. interests. For the uninitiated, sorting out the various recommendations requires a scorecard. For example, at its plenary session scheduled for Melbourne, Australia, in November, the CCITT will adopt very firm Q921 recommendations, says Spusta, but these cover only the protocols known as LapD for Link Access Procedure for the D Channel, which is ISDN's signaling channel. Q931, which addresses the basic function of making and breaking the link between two users, is somewhat further along but will not be sealed in November. As an example, Spusta points out that four bearer services are now defined: voice; 3.1 KHz and 7 KHz for circuit-switched data; and packet-switched data. Still another bearer service might be added, he says. Moving further up the ladder of functionality to the supplementary services such as call forwarding—the Q932 recommendations—will be the subject of the 1988-1992 study period.

SWITCH IN TIME. Yet spirits among ISDN chip makers are remaining high. The time-limiting factor in ISDN's universality is the installation of central-office switches that can handle ISDN signaling—not the CCITT's standards process, says Ron Ruebusch, director of marketing for the communications products division at Advanced Micro Devices Inc., Austin, Texas. "The question is really when ISDN will be ubiquitous enough to give you a good chance of taking a laptop PC anywhere in the country and having an ISDN network available," says Ruebusch. "Then we're talking about the end of the century. There's a lot of equipment out there that has to be changed over. But that is not to say the [near-term] market is not large and attractive. This year, 125,000 ISDN Centrex lines will be installed."

In the race to lock up the growing potential customer base, chipmakers have pushed forward with a program of providing software for compatibility with each central-office switch. AMD will release its AmLink 3 software and development-board package early this month. It will support AT&T's 5ESS, says Ruebusch, and work is ongoing to support

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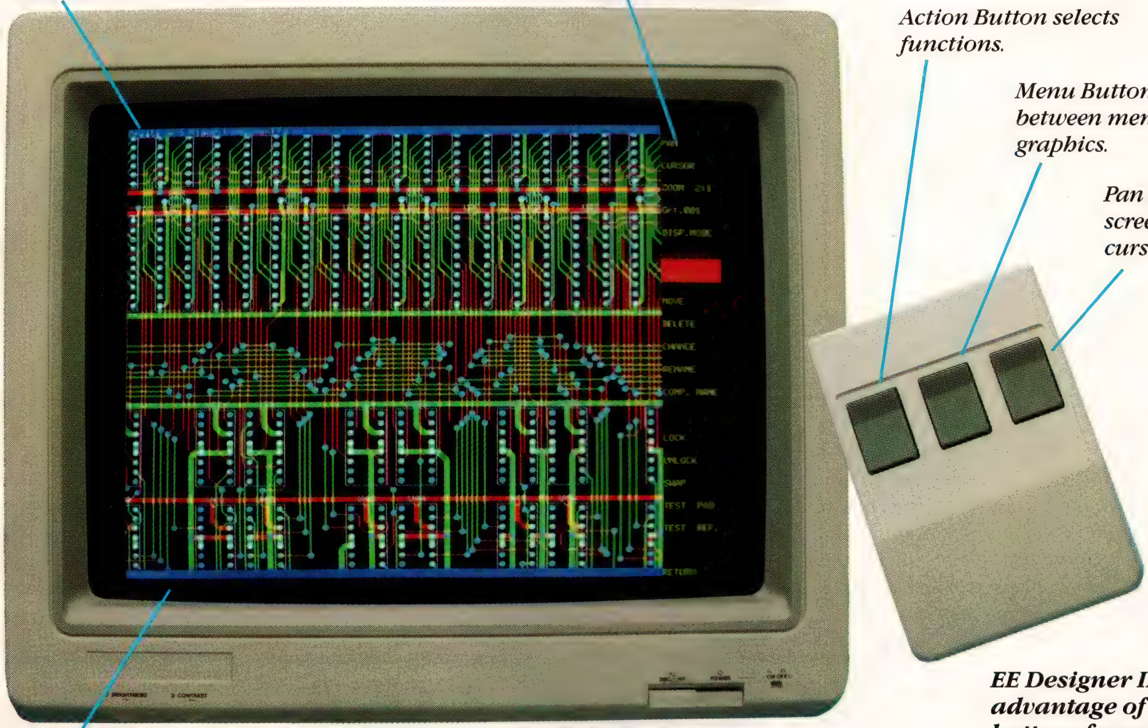

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Northern Telecom's DMS-100. AMD, which developed the software in-house, has had AmLink 3 certified by AT&T.

As has usually been the case in ISDN development, Siemens AG is in the lead with its software offerings, which support both the 5ESS and Siemens' own EWSD switch. Moreover, within the next three months Siemens will extend its software to handle X.25 packet-switched data as well as signaling on the D channel, says Alan Clark, telecommunications marketing manager.

"I hope the switch manufacturers get together," he says, "and Bellcore and the operating companies are very actively pursuing the major ones to do this." But the switch manufacturers spent a lot of time and money developing their products along the lines they think will give them a competitive advantage, he says, and it will not be easy to convince them to adopt an open architecture. For the foreseeable future, however, manufacturers of ISDN customer-premises equipment will probably be implementing the chip software in programmable read-only memory, says Clark, "and once they have it out in the field, they will not be able to change it very readily."

GETTING HELP. Both AMD and Siemens developed their own software, but other major chip makers have turned that job over to a third-party vendor that has long specialized in telecommunications software. AT&T's Microelectronics Division in Allentown, Pa., has opted to handle its software through a third-party vendor that will be announced in the fourth quarter of this year, says Frank Posivak, product manager for ISDN devices. "We've decided customers would prefer a third-party vendor," he says. And Intel Corp., Folsom City, Calif., has teamed up with DGM&S Inc., Mt. Laurel, N. J., for the software to support its ISDN chips.

Taking quite a different tack is Mitel Corp., Kanata, Ont., Canada. "There are an incredible number of proprietary [switch] variations out there that you might have to deal with," says Lou D'Alo, manager for software applications for Mitel's Semiconductor Group. "All have their way of implementing the recommendations as they now stand, and the work needed to implement each one doesn't warrant the release of separate software. We're waiting until the recommendation comes out and the standards are solid."

Despite the formidable obstacles still standing in the way of worldwide—or even nationwide—ISDN services, companies that manufacture customer-premises equipment are taking the plunge. "A lot of the household-name companies are designing or prototyping products, terminals, and subsystems for ISDN," says Siemens's Clark, who adds that much of the activity is in the terminal adapter market.

ISDN HEADS TOWARD FIRMER STANDARDS

ISO Reference Layer	CCITT Standard	Function	Status	Typical Implementation
Layer 1	I431, I431	Physical connection to network	Adopted 1984	Hardware
Layer 2	Q921	Data-link network protocol	Adopted 1986	Hardware/ software
Layer 3	Q931	Basic call setup and teardown	To be adopted November 1988	Software
	Q932	Generic procedures for supplementary services	To be adopted November 1988	Software
		Specific procedures for supplementary services such as call forwarding, caller identification, automatic callback, etc. (voice and data)	Subject of the 1988-92 study period	

SOURCE: *ELECTRONICS*

For example, Hayes Microcomputer Products Inc. of Norcross, Ga., has a PC plug-in board terminal adapter in beta site. At the other end of the user spectrum, Hewlett-Packard Co. is studying the use of ISDN as a backbone for wide area networking applications.

"The idea of worldwide connectivity through ISDN is long way off," says Bob Alley, telecommunications products line manager at the Cupertino, Calif., company, "but there are some applications in which its use will become cost-effective within the near future." *–Jack Shandle*

SOLID STATE

RF LINKS ON A CHIP BID FOR BAR-CODE JOBS

DALLAS

Consider the possibilities. You replace the ubiquitous bar code with radio-frequency links on a chip that can talk with another chip. What you wind up with is two-direction wireless communication that can be used to store, change, and transfer data with little or no human intervention—and even display it on a personal computer's screen. The market potential is vast.

The portable wireless data bases can be updated on-line

That's the happy prospect facing Dallas Semiconductor Inc. The four-year-old company has developed a very-low-power CMOS rf receiver and several other low-power CMOS support circuits and now it is ready to sell both the chips and the systems. The potential buyers are, for starters, those involved in industrial control, manufacturing, hospital-patient monitoring—in short, anyone today using bar codes or paper tags to monitor the changes in people or things.

"At one end of the spectrum it's a dynamic bar code," says Mike Bolan, Dallas Semiconductor's marketing vice president. "And at the other it's a portable wireless data base that can be downloaded to a personal computer." On the bar-code end, it can be attached to an object such as a piece of luggage at an airport. Information about ownership, destination, time of arrival, or time of pickup can be entered and changed as needed. At the high end, the chip could be attached to a truck to record maintenance information and read out on a computer terminal.

Not only that, says Bolan, but the chip can be used with a wide range of coupling techniques. "There's nothing to prevent the use of infrared or microwave, or even acoustic coupling," he points out.

The Wireless family, as it is called, starts with an intelligent base rf transceiver that would typically connect to an RS-232-C serial port on a monitoring station or a desktop computer. On the other end of the rf link are a low-power receiver and a two- to three-wire converter/transmitter support chip plus several other optional support chips. Those chips, along with a 3-V lithium battery, form a self-contained mobile receiver-transmitter that has a working life of 10 years.

Bringing the size down was the biggest challenge in product development. "It can be built by conventional techniques, if you don't care about cost, size, and power," Bolan says, "but if you want it to be inexpensive, small, and to run for 10 years on a lithium battery, then that's where you're facing a tremendous engineering challenge."

–Dave Bursky and Howard Wolff

SEMICONDUCTORS

HOW CASTRUCCI IS PUTTING HIS STAMP ON SEMATECH

AUSTIN, TEXAS

Sematech's Mr. Inside is getting down to business. One month after joining the chip manufacturing consortium as executive vice president and chief operating officer, Paul P. Castrucci is taking his own brand of IBM-style management—"intelligent, pushy, and aggressive," in the words of one former employee—and stamping it on Sematech. He is accelerating the hiring process and already delivering know-how to members.

After 32 years at IBM Corp., all of it in semiconductor research, development, and manufacturing, Castrucci is changing gears for "the opportunity of a lifetime"—the chance to build from the ground up the most advanced bed of semiconductor manufacturing technology the world has ever seen. Although he was originally skeptical that Sematech could work at all, Castrucci is now a converted and devout believer.

"I'm not giving up IBM," he says. "I'm gaining 13 companies and the Department of Defense in this job." But he's also taking over a program that has fallen at least three to six months behind schedule, making it that much harder for it to meet its stated charter: to turn around the decline in U. S. chip-making know-how. Initial plans for Sematech called for prototype chips by this Christmas, but that's out of the question now, because of delays in getting funding from the Defense Department and Congress and in finding top officers to lead the consortium. Now wafers won't be running through Sematech's Class 1 fab until next year's first quarter.

ON THE MOVE. But that doesn't mean Sematech has been dormant, Castrucci says. "You can't analyze this thing like you would a normal fab, where you're manufacturing product," he says. "Knowledge is what we're doing, and we're going to be delivering knowledge before we have wafer starts. We're already doing it: how to design and build leading-edge [facilities] without having to build the very expensive wet-processing buildings we think we need."

The Austin plant, a former Data General Corp. warehouse, is Sematech's first success story. "We took a warehouse and within a matter of nine months turned it into what is probably the leading-edge facility in the world for Class 1 semiconductor manufacturing," Castrucci says. The refurbishing job was also done at minimal cost, although he won't say exactly how much costs were.

Castrucci says Sematech will be the West Point for chip-manufacturing engineers.

Still, members are looking for a lot more than just new ways to build cheaper fabs, and it will be up to Castrucci and chief executive officer Robert Noyce to determine how to develop the three generations of advanced chip-making technology Sematech aims to produce in the next five years. Castrucci says the consortium will draw on members' technologies, such as the 4-Mbit dynamic random-access memory design donated to the project by IBM, on the resources at the national laboratories, on universities, and on strategic alliances with equipment and materials companies. Talks are already under way with several firms, Castrucci says, to develop the manufacturing equipment Sematech will need to produce 0.5-μm technology in Phase 2 and 0.35-μm technology in Phase 3.

Castrucci and Noyce are also trying to fill out their management team as quickly as possible. Castrucci has developed a management plan and is looking for candidates for three key vice presidential posts—manufacturing systems, manufacturing operations, and process development. He is also trying to accelerate the staffing process, both by speeding up new hires and by getting member companies to assign staff three months earlier.

That's part of Castrucci's plan to create an environment that will attract the nation's best talent. "I've said it before, and I really believe this: I want to establish Austin, Texas, and Sematech as the West Point for manufacturing engineers in semiconductors," he says. "The training will be second to none." *–Tobias Naegele*

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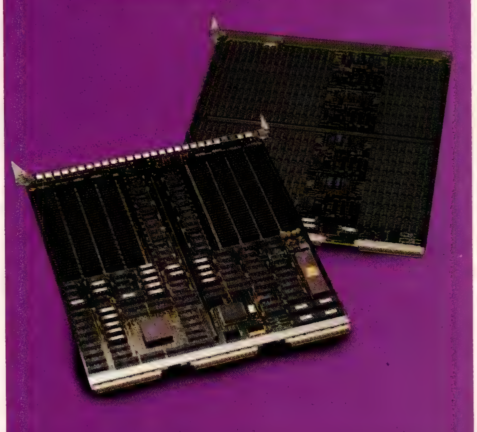

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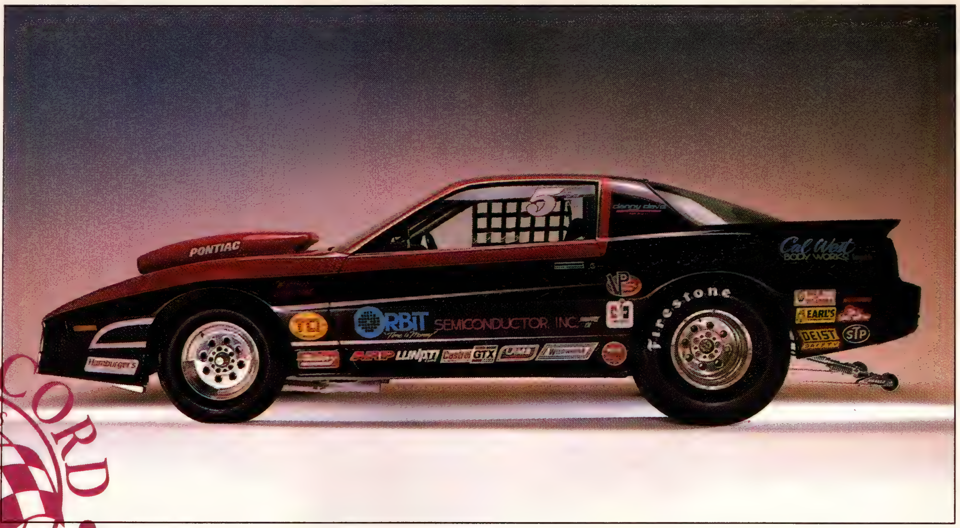

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IN THE PIPELINE: THE FIRST SUN WORK-STATION CLONE

LONGMONT, COLO.

There's a brash new company in Colorado that thinks the world is ready for clones of Sun work stations. And by combining U. S. creativity and design talent with Japanese money and manufacturing prowess, Solbourne Computer Inc. says it's out to accomplish in the work-station market what Compaq Computer Corp. did in the personal-computer arena.

In the coming RISC work-station wars, Solbourne is betting on the Scalable Processor Architecture and the Application Binary Interface proposed as standards by Sun Microsystems and AT&T. And Solbourne plans a machine that will outrun Sun's.

The startup is 52% owned by Japan's Matsushita Electric

Sparc/ABI is one of several approaches that will fight it out in what's expected to be a lucrative market for high-end work stations based on reduced-instruction-set-computer architectures. The worldwide work-station market will grow by 82%, compounded annually, between 1987 and 1991, when it will total $6.3 billion, according to Dataquest Inc., a San Jose, Calif., market-research firm.

Solbourne, a two-year-old startup, announced a Sparc licensing agreement with Sun late in August. At the same time, the firm unveiled a "strategic partnership" with Matsushita Electric Industrial Co. that includes $38.9 million in second-round startup financing. The deal, expected to be concluded in October, brings the total funding committed to Solbourne by its Japanese partner to more than $50 million.

BOTH WAYS. "Matsushita has a majority position [52%] in the company, but we're seeing a great deal of technology flowing in this direction [from Japan to the U. S.] as well as the other way," says Solbourne president Douglas MacGregor. In addition to funding, Matsushita is providing design and engineering support, technology, and manufacturing in exchange for tapping Solbourne's entrepreneurial ingenuity and expertise in high-level chip and system design. MacGregor, before founding Solbourne in mid-1986, was a principal designer for Motorola's 68020, and approached Matsushita with the work-station idea.

Solbourne's first products are expected in early 1989, and will be compatible with the Sun-4 line of Sparc work stations. Those systems will be based on off-the-shelf RISC chips from Fujitsu. But by next year's second half, Solbourne expects to introduce a subsequent generation of machines based on ultralarge-scale integrated circuits in a multiprocessor system design that will be the industry's first Sparc/ABI-compatible work station, says MacGregor.

In the sense that the Solbourne system will run the large software-application library expected to emerge for Sparc/ABI Unix work-station platforms, the system will be the first in a new breed of "Sun clones," MacGregor says. But he claims that the machine will go beyond that to give dramatic work-station price/performance improvements. It could signal "a fundamental change" in the work-station business, he says.

"Just as Compaq came out with the first compatible PC, we're coming out with the first compatible work station," MacGregor says. And just as the emergence of PC clones touched off a competitive market fray that led to the proliferation of low-cost personal computing based on the IBM PC standard, the Solbourne introduction could be the first in a similar onslaught of affordable work stations for the open Sun/AT&T standard, he says.

The Solbourne-Matsushita RISC chip will feature 64-bit-wide data paths, compared to the 32-bit designs of current Sparc processor circuits. It will be fabricated in a Matsushita submicron CMOS process, and integrate about 1 million transistors, combining functions that require several chips in current designs. The Solbourne work-station architecture will support up to eight of the ULSI processor chips working together. In addition, it will be possible to upgrade smaller systems in the field by adding processors.

Solbourne is not talking price or performance specifics. But the focus will be on so-called superwork stations that execute more than 10 million instructions per second. "Our job is to develop computers that will provide superwork station levels of performance at prices that are generally affordable, which means under $10,000," MacGregor says.

Matsushita has marketing rights in Japan, but Solbourne will sell the systems in the U. S., while establishing direct U. S. distribution channels that have eluded Japanese vendors. The two companies will cooperate in marketing to the rest of the world. Beta site and early production models will be made in Japan, but volume manufacturing will be done at Matsushita production facilities in the U. S. *–Wesley R. Iversen*

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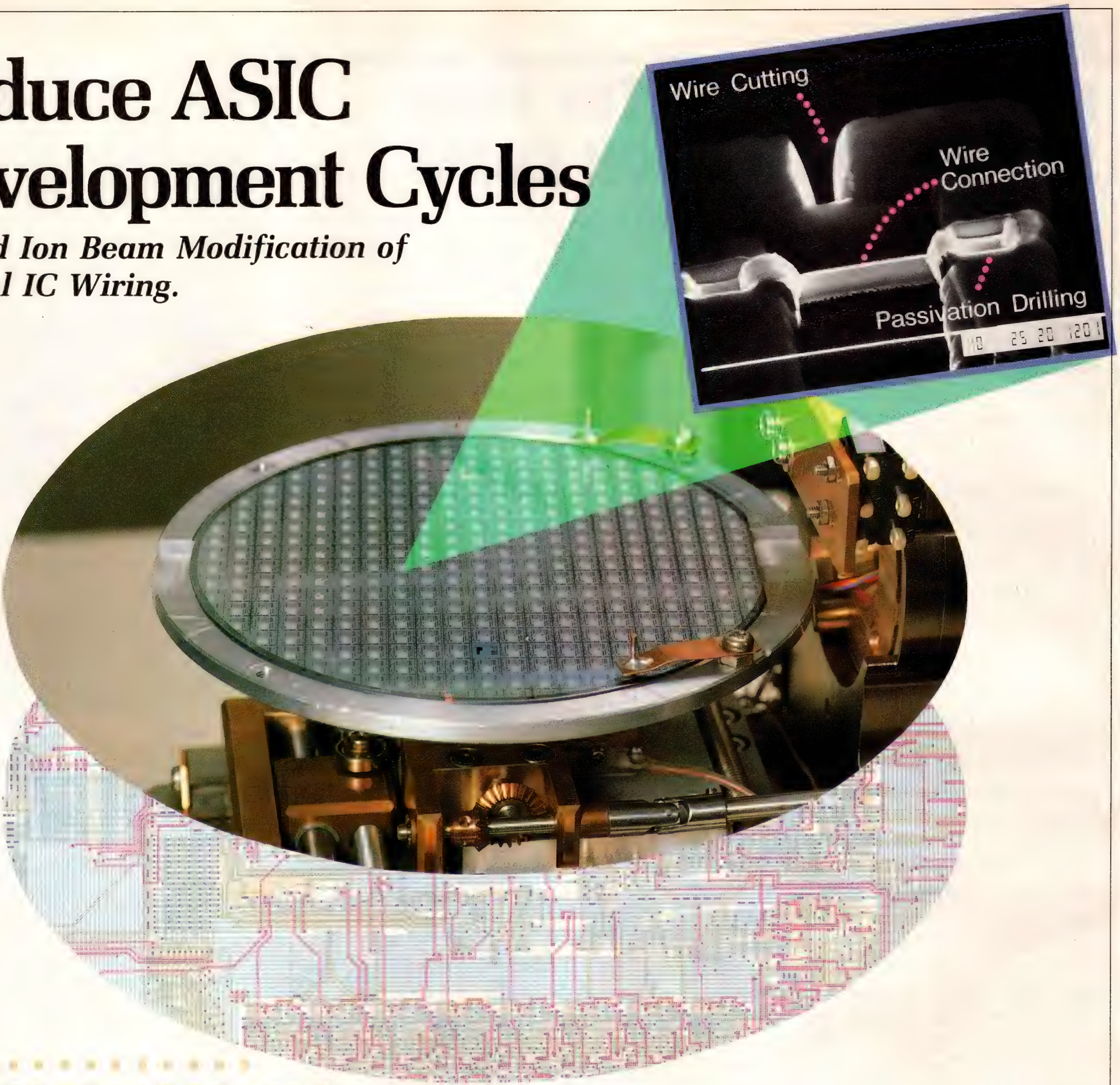

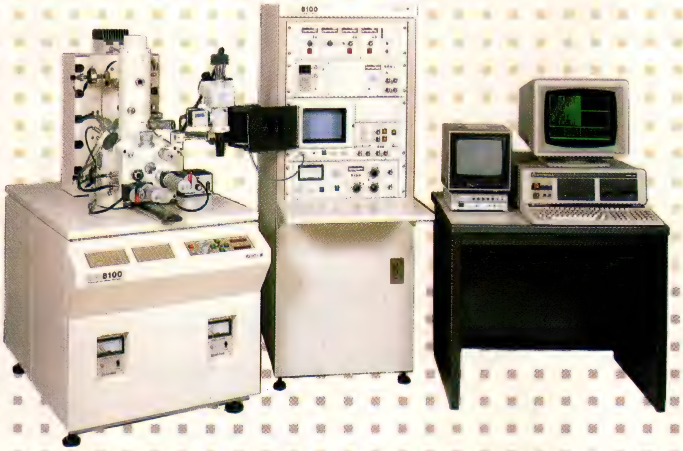

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WILL THE U. S. BE A FOLLOWER IN HDTV TECHNOLOGY?

WASHINGTON, D. C.

The era of high-definition TV is here, and a small crowd of committees, panels, and associations is suddenly scrambling to settle on a standard and get U. S. hardware manufacturers involved. Their ability to do that will determine the future of TV in the U. S.

The Japanese plan to begin broadcasting HDTV signals next year, but it will be a long time before HDTV becomes available in North America. What happens between now and then combines all the tension needed to fire up a burning controversy: the battle over potential standards; the race to establish a standard before one is dictated from foreign shores; and the fear in some industry and government circles that HDTV may be the last chance for the U. S. electronics industry to save its future. The American Electronics Association and some officials in the Department of Commerce and the Office of Science and Technology Policy reason that without a viable consumer electronics industry supporting U. S. chip makers with volume orders, the semiconductor, computer, and communications industries will all be forced off shore.

> What transmission standard should the FCC choose?

The immediate issue facing U. S. broadcasters and manufacturers, however, is which transmission standard the Federal Communications Commission should choose. Japan's MUSE (for Multiple Sub-Nyquist Sampling and Encoding) isn't considered a viable option in the U. S. and Canada because it is incompatible with current National Television Standards Committee guidelines. It is also incompatible with the system used in Europe; to fight off a strong push from the Japanese, European Community nations have developed an HDTV system compatible with Europe's 50-Hz standard.

Compatibility is a big issue in the U. S., too, because of the huge consumer investment in NTSC equipment: Americans own more than 140 million TVs and 40 million video cassette recorders worth a combined $80 billion or more. No one is foolish enough to think that they would be willing to throw it all away in favor of a clearer, brighter, but probably much more expensive picture. The Canadian Department of Communications is also putting compatibility forward as a primary issue, says Matin Akgun, acting director of information processing in the department's Broadcast Technology Branch in Ottawa. He emphasizes that NTSC, which offers 525 interlaced lines at 60 Hz, is used throughout North America, and that any new standard should maintain that compatibility.

The FCC's Advisory Committee on Advanced Television, which is taking the lead in choosing a U. S. standard, has been talking to Canada's Advanced Broadcast Systems Committee and the two are trying to work out a way to divide their labors. The FCC committee is now looking at a range of proposed standards—including MUSE, and systems backed by the David Sarnoff Research Laboratories, Bell Communications Research, the Massachusetts Institute of Technology, and at least a dozen other companies and groups. Formal proposals are due this month, and detailed specifications must be submitted to the committee by December, when testing is scheduled to begin.

The Advanced Television Test Center, a joint venture of the National Association of Broadcasters, the three major networks, and others, was set up this spring to conduct the tests for the FCC. The testing process could take 18 months to a year, says Ben Crutchfield, NAB's director of special engineering projects.

But while broadcasters wait for the FCC to decide on a new transmission standard, the Advanced Television Systems Committee, an industry group in Washington, has already approved a production standard based on the same 1,125-line, 60-Hz output MUSE provides.

NO RUSH. The validity of that standard, however, is in dispute. The NAB, the Association of Maximum Service Telecasters, and nine other ATSC members oppose the production standard because they feel it rushes the issue. Defining how to produce an image before deciding how to get it to the consumer is putting the cart before the horse, says Max Berry, vice president of engineering at the American Broadcasting Co. in New York. "People are saying, first we'll develop a production standard, and then we'll try to get it into the home," he says. "We're trying to do it the other way around."

One complaint about the ATSC production standard is that it's inappropriate for broadcasting because it needs 30 MHz of analog bandwidth for transmission. So it saddles U. S. broadcasters, who are now limited to just 6 MHz of spectrum for each channel, with the burden of figuring

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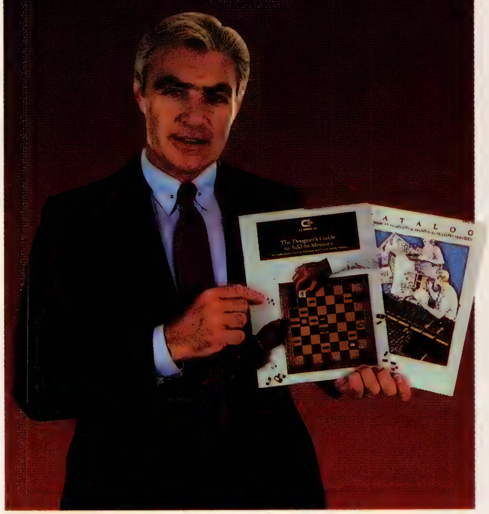

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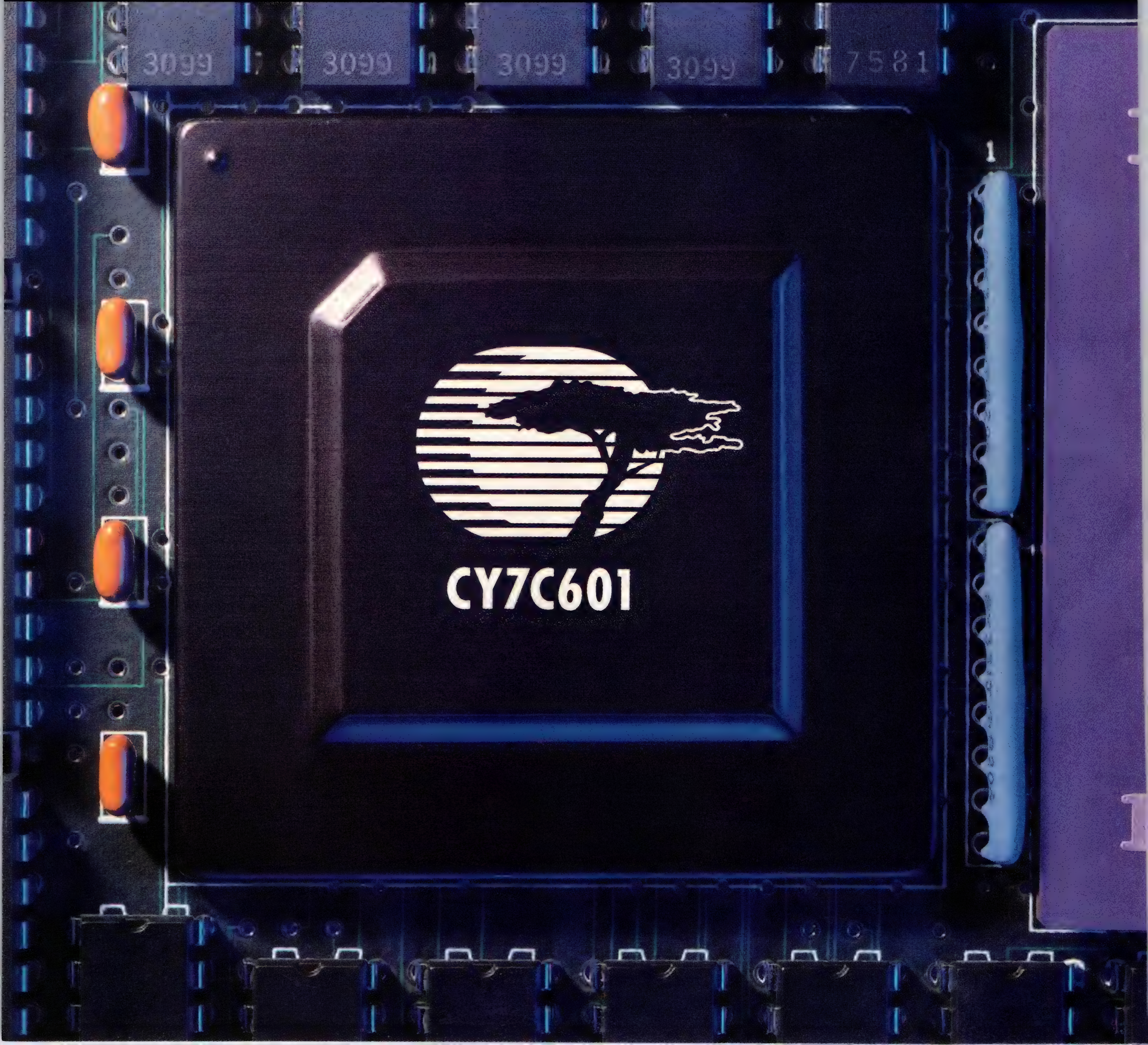

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out how to compress the signal. And while the FCC is willing to allocate new spectrum to terrestrial broadcasters—an additional 3 to 6 MHz per channel has been suggested and would be required by many of the proposed standards—the extra spectrum "may or may not be contiguous," says William Hassinger, the FCC's assistant bureau chief for mass media.

HALF THE SIGNAL. That means broadcasters now transmitting over, say, VHF channel 4 may be given UHF channel 59 to augment their transmissions. But no one is sure yet whether it's possible to broadcast that way, since in many cases viewers may only be able to pick up one channel—half the signal—clearly.

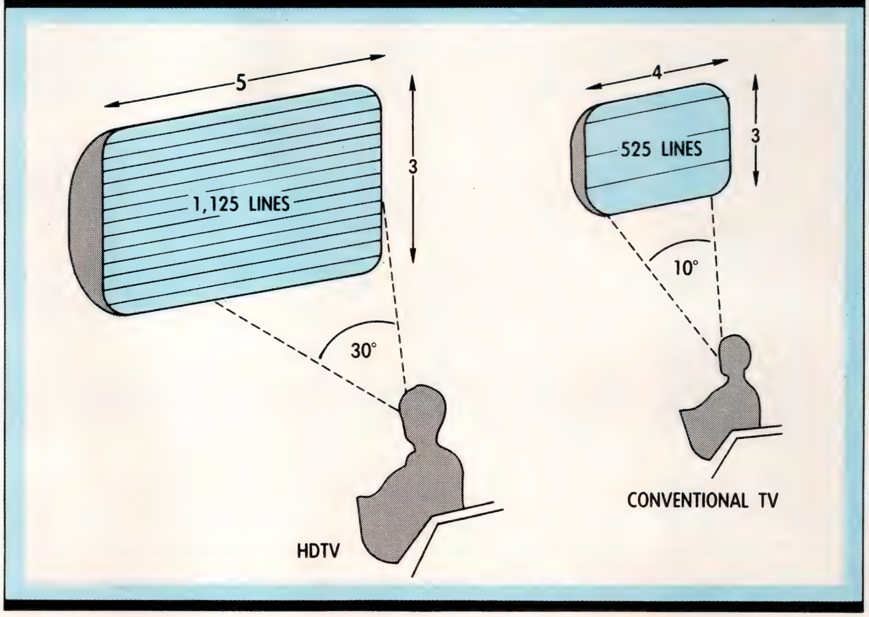
That's one of the issues the FCC will consider before making its decision, Hassinger says. "Our main concern is that broadcasters develop and adapt a system that will keep them competitive—with each other, cable, VCRs, potential direct satellite broadcasters, and with companies that might deliver programming over fiber-optic cable," he explains.

Hassinger's last concern is serious, because it poses a threat not only to over-the-air broadcasters, but also to cable companies. Although presently barred from offering video transmission into the home, the regional Bell Operating Companies are interested in delivering HDTV video into theaters, for closed-circuit broadcasts of live events, for example. Indeed, says one broadcasting insider, "the biggest stockpile of HDTV equipment in the U. S., next to Sony [Corp.]'s warehouse, is at Bellcore." That's Bell Communication Research, the New Jersey-based research and development arm of the seven regional Bell companies. Bellcore is among the firms proposing a standard, and Irwin Dorros, Bellcore's executive vice president for technical services, is chairing the systems subcommittee of the FCC Advisory Committee.

Unlike broadcasters, the regional Bell companies may not need to wait for a U. S. standard to be set before they start marketing HDTV services. Southwestern Bell Telephone in St. Louis, Mo., demonstrated its HDTV capability in August, using the MUSE standard to transmit a Cardinals' baseball game from Busch Stadium to a theater across town.

Southwestern Bell and the other regional companies could deliver these services years ahead of broadcasters because they don't have any spectrum limitations and they don't need to wait for affordable HDTV receivers to hit the market. HDTV displays will have to be much larger than present TVs if the improvement is to be discernible to the viewer, says the NAB's Crutchfield. So present technology essentially offers two options: oversized and expensive conventional tubes or projection systems, which have not fared well with consumers. Alternative flat-panel display technologies have not matured to a point where screens measuring 40 in. or more diagonally are practical.

TV'S NEW ANGLE



An HDTV screen is 25% wider than conventional NTSC sets and offers double the line resolution. The result is a three-fold increase in the viewing angle, from 10° to 30°.

That's where the trade issues come in. HDTV won't take off until the hardware is ready, and that is likely to take another five to ten years, according to most experts. If that's the case, they reason, there may be enough time for the U. S. to mount a concerted effort to redevelop a consumer electronics industry.

"What would it cost for the U. S. to get back into that industry? I don't know, but it will cost us a lot more in the end if we don't do it, " says Pat Hill Hubbard, AEA vice president for technology policy. "If we don't get back into the consumer electronics market with this, the [U. S.] semiconductor industry is going to go offshore for sure."

The AEA is considering asking for federal support of a consortium such as Sematech, the joint industry and government effort intended to revamp U. S. chip-making technology. "It's the issue of competitiveness that we're really talking about here," Hubbard says. "Advanced TV is not just an end market. If we don't do anything, we're headed for foreign domination of both computers and telecommunications." *–Tobias Naegele*

MEMORY

CARTRIDGE-TAPE DRIVES: SALES, BUT NO RESPECT

LOS ANGELES

For a key computer peripheral that has carved out what is becoming a dominant position in backing up disk drives, cartridge magnetic-tape drives get little respect. The Rodney Dangerfield treatment certainly doesn't stem from the industry's solid record, but rather from its lack of product flash—incremental improvements in a known technology don't make much of a stir in the marketplace.

"We're the [electronics] industry's best-kept secret," says D. Howard Lewis, chairman and president of market leader Archive Corp., which pioneered the basic quarter-inch-cartridge tape technology early this decade.

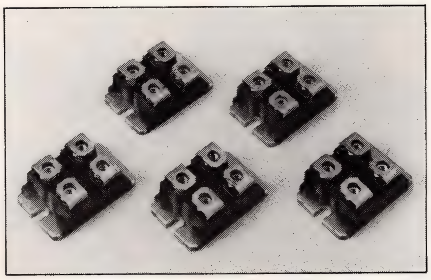
But there's another side to the magnetic-tape-drive industry, belying its image of stolidness. This is a wildly competitive business, with a host of companies jockeying for position in a fray now made more complex by a veritable firestorm of patent litigation.

Since 1982, when only 20,000 cartridge drives were shipped, the demand has been turbocharged: more than 1 million were shipped last year, with a value of $425 million. And this growth spurt is no flash in the pan, says the Santa Barbara, Calif., consultant Raymond C. Freeman Jr. Between now and 1993, "quarter-inch data-cartridge drives will be the big winners in removable data storage on per-

ISOTOP Packages Tailored for High Power Transistors

Besides offering a range of standard ISOTOP-encapsulated PowerMOS and IGBT devices, Philips now offers ISOTOP packages tailored to user requirements. For large orders, PowerMOS, bipolar transistors, diodes and other semiconductor devices can be combined in a single ISOTOP package.

The four-terminal package, which occupies less than 6 cubic cm, can take 50 V devices passing 110 A with drain-source on-resistance of 10 mΩ, up to devices of 1000 V, 0.5 Ω passing 15 A. More rugged and electrically reliable than externally isolated packages with the same power ratings, the package has a single outline for a wide range of power devices and is internally isolated to 2.5 kV RMS for one minute.



ISOTOP Powerpack tailored for user requirements

The package can be mounted on a printed circuit board. It has very low internal lead inductance and capacitance, and good thermal resistance between junction and mounting base. The package has screw terminals.

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Rugged Logic-Level MOSFETs Accept 5 V Drive Voltages

A range of logic-level MOSFETs from Philips Components has guaranteed gate-source breakdown voltages of 15 V, rather than the industry standard 10 V. The BUK500 range includes devices that also withstand drain-source voltage spikes of up to 400 V, making them the most rugged logic-level MOSFETs available. The transistors can replace mechanical relays, with drain-source on-resistances down to 40 mΩ, allowing them to pass currents up to 40 A (A 30 mΩ device is currently being developed). They are driven into full saturation by a 5 V gate source, making them ideal for automotive and industrial applications.

The family consists of 14 transistors with maximum drain-source voltages of 50 V, 100 V and 200 V. Depending on crystal size and package, current ratings vary between 12 A and 40 A for the 50 V devices, between 8 A and 25 A for the 100 V devices, and between 5.3 A and 12 A for the 200 V devices. Switching times are comparable to those of standard MOSFETs.

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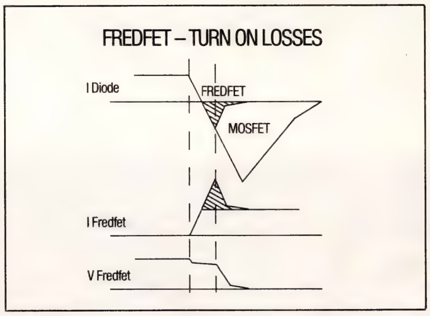
The transistors come in three packages with different power ratings: the TO186, dissipating up to 30 W; the SOT82, dissipating up to 75 W; and the TO220, dissipating up to 125 W. Samples are available.
A 150 W, 30 mΩ device is in development.

Circle 811

FREDFETs Reduce Commutation Losses in Bridge Applications

Aimed at half- and full-bridge applications, these 13 FREDFETs combine commutation losses between five and ten times lower than standard MOSFETs with excellent dV/dt behavior. Each member of Philips Components' BUK600 family has an integral Fast-Reverse Epitaxial Diode that offers significant advantages at frequencies greater than 50 kHz in circuits for motor control, inverters and uninterruptible power supplies.

By doping the epitaxial layer of a standard MOSFET, a FREDFET transforms the inherently slow parasitic reverse-biased diode between a MOSFET's source and drain to a fast one. This reduces the device's stored charge, and hence the reverse recovery time by a factor of five or more in practical circuits to as low as 125 ns for a 500 V, 11 A device at 25 °C junction temperature. The doping also keeps leakage currents and drain-source on-resistance down to those of other PowerMOS devices.



Turn-on losses: MOSFETS vs. FREDFET

The BUK600 family has maximum drain-source voltages between 400 V and 1000 V, while drain-source on-resistances as low as 0.4 Ω lead to high drain currents of a maximum of 14 A for the 400 V transistor and nearly 9 A for the 1000 V devices. Larger crystal sizes will be introduced in early 1989.

The BUK600 devices come in TO220, SOT93 and SOT199 packages. Samples of the 400 V, 500 V and 600 V devices are available now. Samples of the 800 V and 1000 V devices will be available early next year.

Circle 812

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Philips Components

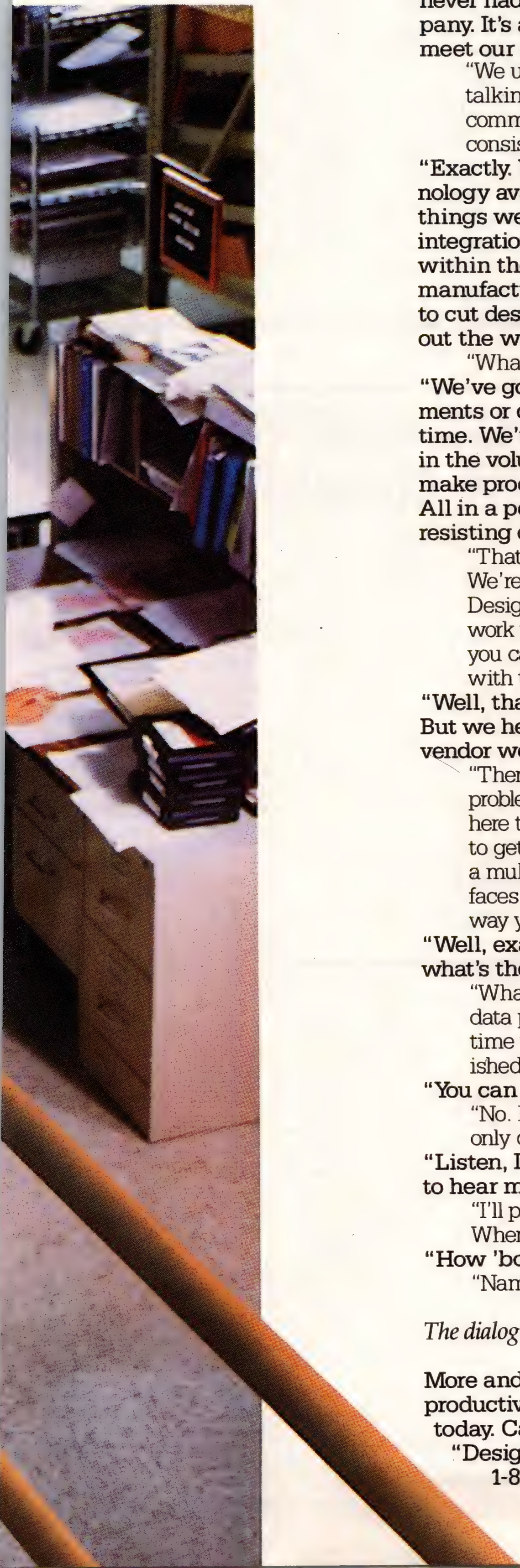
PHILIPS

PHILIPS

Circle 813

"By the time we got this product out, our competition had been there 5 months. We figure it cost us $3 million in sales."

"I remember when you were always out there *first.* Tell me what's happened and let's see how HP DesignCenter can help speed up your whole process."



we never stop asking

"What if...

"I think we've got a pretty good handle on why we seem to be lagging behind. We have too many prototype revisions before we get out of the lab. And each one takes time. It's that simple."

"We hear that from a lot of our customers these days. And development time isn't the only problem."

"You're telling me. Our markets are changing pretty much by the month. It's moving so fast and we've got to be able to react. This whole environment is creating all kinds of demands on us we've never had before. In every department in the company. It's absolutely essential that we find ways to meet our schedules for new product introductions."

"We understand those demands at HP. You're talking about resource constraints, cost and time commitments, limited R&D funding, product consistency, that kind of stuff, right?"

"Exactly. We need to make better use of the technology available to us. Let me tell you about some things we need to do. One that's critical is logical integration, not just physical, between groups within the company–design, test, mechanical, manufacturing–so they can work more closely to cut design time without letting quality go out the window."

"What else?"

"We've got to be able to make product improvements or develop entirely new lines at the same time. We've got to handle a tremendous increase in the volume of code we're writing. We've got to make products manufacturable on the first pass. All in a people environment that is notorious for resisting change."

"That's why we need to talk about DesignCenter. We're not talking about equipment alone. DesignCenter gets at the issues of how people work together, how you hold your profit line, how you can deliver products on time and still lead with technology."

"Well, that's what we *need* to be talking about. But we hear this productivity story from every vendor we talk to. What makes HP any different?"

"There's simply nobody out there that looks at the problems you're facing today like we do. We're not here to sell one 'better box' after another. We're here to get involved–to be a partner. We'll help design a multi-vendor system that works, customize interfaces, train your people . . . until you're running the way you need to be. We're that serious."

"Well, exactly what is DesignCenter? I mean, what's the bottom line, what does it mean to us."

"What we're trying to do is give your people a single data path–plus all the support you need–from the time you come up with an idea through to a finished product. I mean out the door and on the truck."

"You can do that today?"

"No. Nobody can. But the fact is, HP is probably the only company that can get you there any time soon."

"Listen, I want some of our project managers to hear more about DesignCenter."

"I'll put a team together and call you tomorrow. When do you want them here?"

"How 'bout Thursday?"

"Name a time."

The dialogue continues . . .

More and more companies are talking to HP about productivity and DesignCenter. Start a dialogue today. Call toll free and request the free booklet "Design Automation . . . The Bottom Line."
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Circle 39 on reader service card

hp HEWLETT PACKARD

sonal and midrange computer systems," he says, with sales growing 15% a year. The biggest winners, says Freeman, will be the 3.5-in. drives now on the drawing board in the 150-Mbyte-and-up range.

Archive, of Costa Mesa, Calif., has consistently been No. 1 in the market, last year grabbing 26% of the business, says Freeman. Next is the Wangtek subsidiary of Rexon Inc. in Simi Valley, Calif., followed by Irwin Magnetics Systems Inc., Ann Arbor, Mich., and Cipher Data Products Inc., San Diego.

All of them are working with a proven, familiar technology that keeps offering the larger capacities and smaller package sizes that customers want. The flip side is that such improvements are not exciting enough to stir much enthusiasm, so the business appears to be easy pickings for new technology.

Indeed, the industry has successfully fought off challenges from such ballyhooed technologies as erasable optical disks and digital audio tape, and before them, from higher-density floppy disks and removable hard disks. One reason is that learning-curve improvements and economies of scale keep cartridge costs low—currently, under $3 per megabyte. By contrast, erasable optical disks, whenever they hit the market, would set users back twice that much, he says.

But if the alternative technologies don't appreciably dent the industry's fortunes, the patent issues might. At center stage is Archive, which says it developed the fundamental technology on the quarter-inch streaming-cartridge tape drive some eight years ago. At the time, "we felt strongly [that the technology] was not patentable," says Lewis, so the company did not apply. Cipher did—"they came out of nowhere," Lewis complains—and got one.

NOT EXPECTED. The saga began in 1981 when Archive licensed Cipher to build its cartridge, with the proviso that any improvements be disclosed by both sides. In 1982 Cipher filed a patent application that covered loading the tape cartridge, opening the door, and moving the head to contact the tape. Archive says it was not informed, so the company was stunned when Cipher won the patent in 1986. Cipher meanwhile signed Tandberg Data A/S of Norway to a licensing deal and sued Wangtek for infringement.

The pace really quickened last May when Archive filed suits against Cipher, charging misappropriation of trade secrets and seeking to invalidate the patent. Cipher counter-sued for infringement. Further complicating things, Wangtek suddenly settled with Cipher, for $3.4 million and future royalties.

While no one is predicting the outcome of the Archive-Cipher suits, until they are settled the business will be laboring under a legal cloud. *–Larry Waller*

IN TAPE DRIVES, BUSINESS IS STEADY

(UNITS IN THOUSANDS)

MINICARTRIDGE	1987	1988	1989	1990	1991
< 5 Mbytes	8.7	8.0	3.6	1.0	0.0
5 to 30 Mbytes	135.7	93.0	52.0	37.0	11.0
> 30 Mbytes	255.5	517.4	780.0	1,020.0	1,240.0
Total	399.9	618.4	835.6	1,058.0	1,251.0
CARTRIDGE					
< 20 Mbytes	19.7	15.5	9.0	3.2	1.0
20 to 80 Mbytes	583.4	547.4	459.0	339.0	210.1
80 to 250 Mbytes	55.1	195.9	306.0	436.0	475.0
>250 Mbytes	0.0	0.2	20.0	70.0	205.0
Total	685.2	759.0	794.0	848.2	891.1
Total Drives	1,058.1	1,377.4	1,629.6	1,906.2	2,142.1

SOURCE: FREEMAN REPORTS

PERIPHERALS

HERE COME DISK CONTROLLERS AS FAST AS THE COMPUTERS

NEW YORK

The long winter of the high-speed Intelligent Peripheral Interface is just about over. This standard for use in disk- and tape-drive controllers was enacted nearly five years ago but is just coming into use because the drives that run fast enough to use IPI's speed advantage have been delayed. Now a boom seems to be building as disk-drive manufacturers are preparing to market complete storage subsystems that are based on IPI.

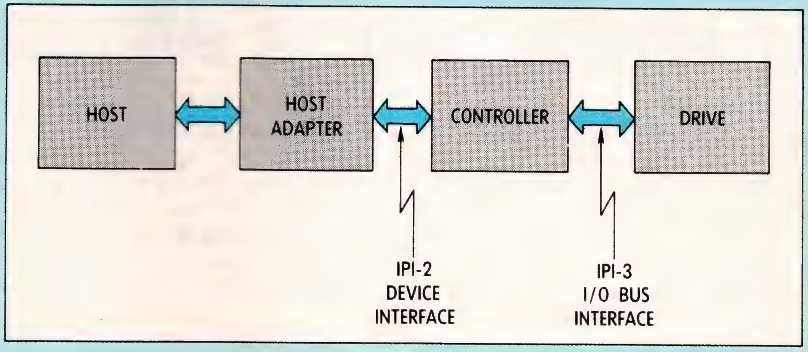
> The standard has been waiting five years for speedy drives

Speed is what IPI is all about. Today's computer systems—built with fast processors, incorporating multiple parallel processors, and using high-performance graphics—must receive data faster than the Storage Module Drive, the most common drive interface used in high-end systems, can deliver it. Without the fast drives, IPI was a solution in waiting. But now, as the demand builds for IPI speeds and as products become available, the market should start to bloom. What's more, because IPI has just started climbing its technology curve, enhancements are inevitable. "This is the year that IPI finally comes of age," says Chappell Cory, senior vice president of marketing operations at Xylogics Inc. of Burlington, Mass., a leading controller makers for open buses.

That may well be, but for the present, it's impossible to know just how high the market demand might reach. The market for IPI drives and controllers is just too small to measure, and will be tough to call for a while. The biggest excitement is in what one analyst calls the IPI-3 market. Three types of products are included: external IPI subsystems, IPI-2 drives integrated into computer systems, and drive strings connected to an IBM Corp. IPI-3 host interface. This segment "is beginning to be significant," says Dal Allan, consultant and principal at ENDL in Saratoga, Calif., although he believes that the IPI-2 market will remain very small for the next couple of years. "IBM alone has shipped more than 125,000 spindles of IPI-3 drives [IBM puts IPI drives on its 9370 midrange systems], and that does not include IPI tape drives," says Allan. He also points out that Tandem and Siemens are selling computer systems with IPI drives and that NEC Information Systems, Hitachi, Control Data, and Fujitsu are selling IPI-2/IPI-3 subsystems.

Right now, IPI puts out up to 10 Mbytes/s, well above SMD drives and controllers, which reach a transfer rate of up to 3 Mbytes/s. Although the Small Computer Systems Interface is fine for the bottom end, only IPI can satisfy the voracious appetites of high-end computer systems and super work stations. "IPI is very important to the computer industry because it is the way to get higher data rates," says Xylogics' Cory. "We are expecting a lot of demand for IPI to show up now—a lot of our customers want it.

WHERE THE INTERFACE FITS IN



A two-stage interface can be implemented with the high-speed Intelligent Peripheral Interface, as shown, or an IPI-2-based interface can be built to plug directly into a host bus.

In the late 1970s system designers who saw a way to solve some tricky integration problems of the future started work on concepts that led to IPI. But "the real work [on defining an IPI standard] began about 1981 and it was finished, complete with documentation, in 1985," says consultant Allan. "Since then, fast drives have been the critical missing link for use of the IPI interface; we thought five years ago that they would be here next year," he adds.

The standard covers two levels of peripheral interfaces. The IPI-2 is the device interface between the controller and the storage device. The IPI-3 specifies the input/output bus interface between a peripheral controller and the host adapter that connects to the computer system bus. Both handle 16-bit parallel transfers.

Besides speed, IPI offers a number of other advantages. One is a simple single-cable system, which can be as long as 65 meters. Another is that IPI can relieve the host computer of detailed device commands, such as seeking, searching, and transferring data, thus freeing it to issue only high-level commands, such as read and write.

MORE THAN SPEED. In addition, an intelligent controller can handle defect management by performing such functions as error detection and correction, retries, and the isolation of storage media flaws through sector reallocation, without any intervention from the host. Intelligent controllers can also do automatic configuration of multiple peripheral devices serving multiple hosts, and they can perform extensive diagnostics on the input/output subsystem.

On the product front, four major disk-drive manufacturers are getting IPI drives ready and three computer companies are selling systems with IPI drives. Control Data Corp. is announcing a 6 Mbyte/s drive this month and is currently developing a faster IPI controller that will run disk drives in parallel. To build this drive, the Minneapolis company took the top of its five-product Saber line, a 1.2-gigabyte drive, and changed it to read and write from two heads in parallel for a data-transfer rate of 6 Mbytes/s.

In addition to Control Data, disk-drive vendors Fujitsu America, Hitachi, and NEC are selling packaged subsystems using IPI-2 and IPI-3. Their next fast products will be disk drives for original equipment manufacturers.

NEC is working on a drive with increased track density to hit a speed of 4 Mbytes/s, to be introduced in late 1988 and available in early 1989. For its part, Fujitsu America "is very committed to IPI-2 and IPI-3, both for the OEM market and some captive products," says Anil Vasudeva, director of storage-system products at the San Jose, Calif., division. The company has IPI products on the market and some new ones are waiting in the wings.

Now that the faster drives are here, the controller companies are getting busy, too. Interphase Corp., one of the leading vendors of peripheral controllers for Multibus and VMEbus, is announcing an IPI controller for VMEbus. The new V/IPI 4260 Cougar, due in the first quarter of 1989, offers the performance and convenience of IPI features to the large number of VMEbus system builders.

The Cougar is based upon a second-generation 32-bit internal version of Interphase's BusPacket technology, which was designed for realizing bus transfer speeds nearly up to the maximum of the VMEbus. The newest BusPacket delivers up to 38 Mbytes/s over the VMEbus—95% of its 40 Mbyte/s top speed. This new controller is an IPI-2 master targeted as a disk controller. It follows the IPI-2 device interface standard on the drive side. On the other end the $4,995 board connects directly to the host system bus and does not use the IPI-3 host adapter interface.

Four major drive makers are ready with IPI-based units

Interphase did not use any of the IPI chip sets currently available, because "none could fit our needs," says Ernie Godsey, product marketing manager. Instead, it developed its own IPI I/O control processor using a gate array, and incorporated a MC68020 to do the rest of the intelligent control functions.

Xylogics, the second of the three big companies in the controller business, has also been active in IPI. "IPI-2 is just around the corner and it is time for systems companies to start designing in it and using it," says Cory of Xylogics. "Xylogics is fully committed to high-performance IPI controllers and will be announcing products this year," he adds.

Unlike its competitors, the third major controller maker, Ciprico Inc. of Plymouth, Minn., does not think the time is yet ripe for IPI. "We have done some looking at IPI and we started development on an IPI product early this year; but we put it on hold for a product cycle or two," says Bill Moran, product manager. He reasons that an IPI controller today offers no data-transfer speed advantage over SMD because the available drives limit the speed. That will change eventually, he adds, because "4.5-Mbyte/s drives are coming some day." In addition, he says, IPI controllers are pretty high technology and therefore take a lot of development time and money. As a result, they will cost more than SMD and SCSI controllers. Not only that, but Moran says that Ciprico believes SCSI and SCSI-2 are gaining a lot of momentum right now, perhaps even at the expense of IPI.

"Sure," responds Interphase's Godsey, "IPI controllers will not give performance much better than that available with SMD, using the old drives." But IPI is starting where SMD is finishing and the faster drives are coming, he says. "So we think it is better to be ready for the demand for faster data rates from secondary storage when it starts to explode."

The IPI interface is just starting its technology climb as well. The IPI committee is now working to double the clock speed of the IPI-2 interface to raise the transfer rate to 20 Mbytes/s. Another version of IPI with a wider data path is also in the works. It will use a second cable, but the protocol will remain unchanged. A dual-cable version of SCSI takes a similar approach. In addition, work is now being done to put both SCSI and IPI on fiber-optic links. All these developments could lead to data-transfer rates above 100 Mbytes/s in a few years. So the question is whether drive makers will keep pace, developing drives that can make use of such rates. *–Tom Manuel*

BIPOLAR

SURPRISES ARE THE RULE AT ANNUAL BIPOLAR MEETING

SAN JOSE, CALIF.

In the three years of its existence, the Bipolar Circuits and Technology Meeting has never fallen short in its ability to produce surprises at both the circuit and process level. And this month's meeting in Minneapolis, Minn., is no different.

As in previous years the meeting will produce an array of analog and digital bipolar standard and semicustom circuits and methodologies that break records for performance. But the real excitement is on the process side, with several key papers on alternatives to junction isolation and dielectric isolation. The new techniques offer the promise of higher voltage power transistors and ICs, higher performance bipolar logic, and monolithic microwave ICs that rival gallium arsenide in their performance.

Papers from Digital Equipment Corp., Motorola Semiconductor, Purdue University, and the Massachusetts Institute of Technology take divergent approaches to achieving the electrical characteristics of dielectric isolation in high-frequency bipolar logic, monolithic RF applications, and power-transistor implementations.

Researchers from MIT and DEC have taken their cue from the use of selective epitaxial growth in submicron CMOS to isolate transistors, reduce second-order effects, and achieve higher densities. They have developed a semi-dielectric device-isolation technique for bipolar transistors.

They have overcome a weakness that has limited selective epitaxial growth in its application to bipolar transistors: defective regions at the edges of the epitaxial islands lead to higher leakage currents and lower breakdown voltages. The team has come up with a process that combines selective epitaxy, standard local oxidation, and a shallow buried layer to achieve a semi-dielectric device-isolation structure that uses a mesa etch to eliminate the defective regions.

Tek and Rensselaer have a 12-chip fast RISC set that handles 250 mips

A related technique, epitaxial lateral overgrowth, has been used at Purdue University's School of Electrical Engineering to build a quasi-electrically isolated power transistor in which the transistor is isolated laterally, with an oxide, and vertically, partly with a junction and partly with an oxide. Compared to traditional dielectric isolation, the structure dissipates heat better through the single-crystal silicon and is less complex, resulting in potentially higher yields.

Alternatively, looking for a way to achieve lower costs as well as higher performance in silicon-based monolithic microwave integrated circuits, engineers at Motorola Inc.'s Semiconductor Products Sector in Phoenix, Ariz., have turned to a modified silicon dielectric isolation technology that resulted in transistors with toggle frequencies as high as 8 GHz, more than matching the performance of GaAs equivalents. The designers built a 900-MHz three-stage power amplifier capable of 24 dB of gain at 0.25 W.

On the circuit-design front, the good news is that silicon bipolar is alive and well. A case in point is the remarkable throughput that a team from Tektronix Inc. and Rensselaer Polytechnic Institute has been able to achieve with its 12-chip fast reduced-instruction-set computer. Made with an advanced bipolar ECL process under development at Tektronix, in Beaverton, Ore., the chip set is capable of 250 million instructions per second, about 20 to 25 times the throughput of any of the RISC machines now available.

In a bid to push bipolar ECL SRAMs beyond the current 64-Kbit density level without sacrificing performance, researchers at Motorola's bipolar technology center in Mesa have developed a memory technology employing a single polysilicon layer for all device electrodes, resistors, and load elements and uses diodes instead of Schottky-type cells as the load elements. The 1-Kbit SRAMs initially developed as an evaluation vehicle have achieved access times as low as 3.5 ns and have dissipated only 500 mW.

Finally, a team at Hitachi Ltd.'s Central Research Laboratory has developed a FET pull-down technique that overcomes one of the major limitations of ECL circuits, a drastic decrease of the load delay with a decrease in the drive current. Instead of using npn or pnp devices in the emitter-follower circuitry, the researchers have used FETs for an improvement of three to five times in current-drive capability, and an improvement in overall performance. *–Bernard C. Cole*

DISTRIBUTION

FINALLY, DISTRIBUTOR COMPUTER PROFITS

LOS ANGELES

It took more than a decade, but electronics component distributors finally have figured out how to sell computers at a profit. If the trend holds up, it could signal a major change for the distribution industry.

As the likes of industry-giant Avnet Inc. and regional-operator Wyle Laboratories Inc. lead the way, they pioneer what appears to be a reorientation of parts distribution away from overdependence on semiconductors and the accompanying feast-or-famine business cycles. In the past, chips have made up the vast bulk of all distributor sales. But if the new direction turns out to live up to industry hopes, the computer portion of distributors could approach 50% by the mid-1990s, industry watchers predict.

It is no surprise that the early leader is Avnet, whose Hamilton/Avnet operation in Culver City, Calif., has led the way in so many segments of distribution. Its computer-equipment sales for fiscal 1987 were $400 million, of $1.8 billion total revenue, and could top $500 million this year. But Avnet shares the spotlight.

GOING NATIONAL. Also a factor is Wyle Laboratories Inc., a Western regional distributor, which sold $120 million in computers in 1987 after selling just $42 million worth in 1986. Now it has taken a bold jump into the highly visible Northeast by opening three outlets intended to sell computers to business users, thus going national for the first time. The company expects computers to make up half its projected $1 billion revenue by 1994.

The key attraction of serving business customers with computer equipment is the vast potential, compared to the potential in the chip market, agree Anthony R. Hamilton, Avnet chairman, and Charles M. Clough, Wyle chief executive. Distributors are bumping against growth limits in the $16 billion U. S. chip business, where they account for nearly 30% of the total. Despite today's semiconductor boom, intense competition caused by chip manufacturers awarding too many distribution franchises has cut margins to the bone. And though the top distributors are doing well, annual growth prospects are nowhere near the 20% level that was the rule not too many years ago.

By contrast, end-user sales potential for computers, peripherals, and software amounts to something in the $100 billion neighborhood, more than six times the maxell®

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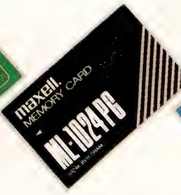
ML-1024PG

EO-128PC

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Circle 51 on reader service card

size of the chip market. Appealing to the aggressive distribution executives even more is the fact that there are few sizable competitors blocking the way of large national companies that can supply a customized computer setup assembled from a broad line of choices by experts.

"It looks like it's wide open to the expertise we bring to the party," notes Clough. And the growing success leads him to add, "they said we couldn't do it, but they were wrong."

Richard Shaffer, a computer-industry watcher, agrees that distributors can prosper in this field, but they are still largely unknown to users and must prove themselves. "There's always room for another good [sales] channel," notes Shaffer, the editor of New York-based Technologic Computer Letter. Profitability should not be an insurmountable hurdle for a well-run entity, he says, "because if you can make money selling those [component] parts, you can make it [with computers]."

DIFFERENT ANIMALS. Now that there's light at the end of the tunnel, distribution veterans say they couldn't have gotten to their position without the experience gained in hard times. They learned they couldn't tie the computer and component businesses too closely. "We hired a computer expert and put him in the midst of all those semiconductor veterans and it just didn't work," says one official.

Matt Crugnale, principal at marketing consultant Crugnale & Associates in Mountain View, Calif., sums up the dilemma by saying, "The losses of the past in fact relate to a serious mismatch between the skills of industrial distribution and the trade practices of the computer industry." In essence, users of computers do not buy them in the way original-equipment manufacturers buy chips, and they never will, observes Crugnale. It is the difference between ordering standard commodities in the hundreds of thousands and buying fewer, more complex items that from the first contact require very close customer service ties. Any chance of succeeding requires splitting computer sales off entirely and controlling costs so break-even points are lower, Crugnale says.

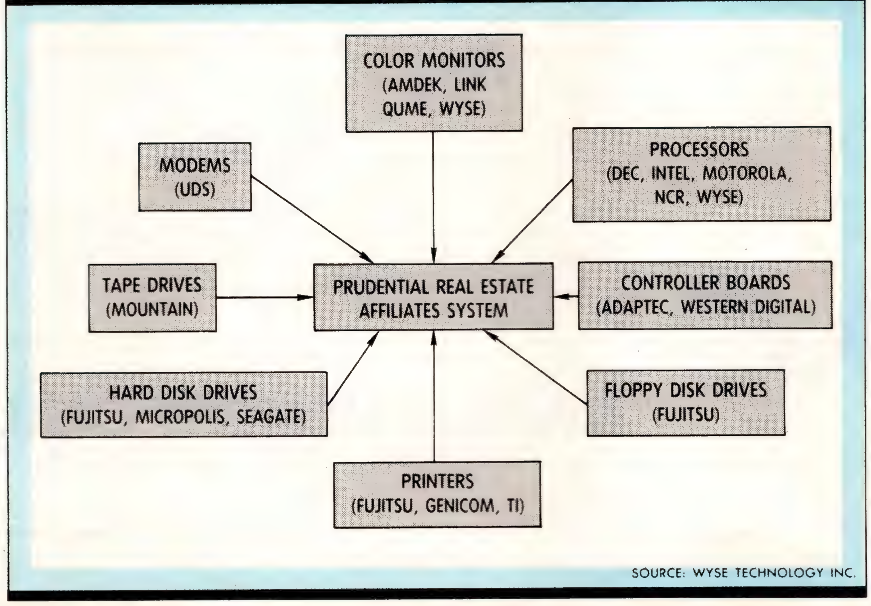
That's what Avnet and Wyle have done. "They are completely separate profit-and-loss units," says Hamilton, because "we want to concentrate on the products." While margins at Hamilton/Avnet Computer run lower than in chips, about 20% against nearly 30%, growth is faster. The higher volumes in sight should improve them. Avnet is targeting $1 billion in computer sales by the early 1990s.

Distributors are also finding that customers like having a broad range of computer and noncomputer products available. Other sources—direct sales forces of manufacturers, value-added resellers, and retail computer stores—have less to offer buyers, all of whom have different needs. One example is Wyle's Prudential contract, the company's initial multimillion-dollar sale, for systems that could be assembled only by a mix-and-match process (see figure). "It's not modeled after the chip business at all; we don't need the same number of bodies," notes Josh Napua, executive vice president for Wyle's computer products organization.

Because they are selling to the broad range of computer users, there is little advantage to being known as part of a distribution firm, "so we want to get away from the distributor tag," says Napua. Wyle's profit margins are at 20% and growing, with about half its sales in Digital Equipment Corp. gear. Avnet is a major DEC outlet also.

Because computer sales offer faster growth than chip sales, distributors who want to keep up with leaders Avnet and Wyle had better get cracking, warns computer analyst Michael Gumport of New York's Drexel Burnham Lambert Inc. "It's scheduled to be a big couple of years [ahead] and it is a make-or-break story for all of them," he says. *–Larry Waller*

HOW ONE SYSTEM WAS CUSTOMIZED


COLOR MONITORS (AMDEK, LINK QUME, WYSE)
MODEMS (UDS)
PROCESSORS (DEC, INTEL, MOTOROLA, NCR, WYSE)
TAPE DRIVES (MOUNTAIN)
PRUDENTIAL REAL ESTATE AFFILIATES SYSTEM
CONTROLLER BOARDS (ADAPTEC, WESTERN DIGITAL)
HARD DISK DRIVES (FUJITSU, MICROPOLIS, SEAGATE)
FLOPPY DISK DRIVES (FUJITSU)
PRINTERS (FUJITSU, GENICOM, TI)

SOURCE: WYSE TECHNOLOGY INC.

Distributor Wyle demonstrated the power and flexibility of its mix-and-match approach in the computer system it put together for sale to Prudential; the final ingredient is service.

RESEARCH

WILL 1989 SEE EUROPE'S CHIP CO-OP TAKE OFF?

HAMBURG, WEST GERMANY

Europe's drive to match the U. S. and Japan in semiconductor technology by the mid-1990s should move beyond the planning stage early next year. The step intentionally dovetails with the planned addition of new corporate members who will provide some much-needed financial backing.

Over the course of eight years the Joint European Submicron Silicon project (Jessi) could spend up to $3.5 billion of corporate and government money to develop technology to implement the high-density, high-complexity memory processes with 0.3- to 0.4-μm features—with intermediate steps for logic applications. Although interest is focused on the project's role in developing this advanced manufacturing technology, Jessi has a more ambitious goal. It also aims to develop standard design tools for future logic devices featuring up to 10 million transistors per chip.

TECHNOLOGY DRIVER. As with other major semiconductor ventures, the technology driver is memory—in Jessi's case the 64-Mbyte dynamic random-access memory. In addition to this technological challenge, Jessi's planners must also wrestle with the tricky problems of choosing a European headquarters and finding a wellspring of technology talent.

So far, experts from Philips of the Netherlands and West Germany's Siemens AG have been calling the shots on the planning team. But Hans Weinerth, representing Philips' German unit on Jessi's advisory board, says he is confident that others, specifically the Italian-French combine SGS-Thomson Microelectronics, will soon join the party. Weinerth, 53, is a director of Philips' Hamburg operations and head of the technology de-

TECHNOLOGY IN HOLLAND

Telecommunications Industry Update

A REPORT FROM THE NETHERLANDS FOREIGN INVESTMENT AGENCY

In 1989, the Netherlands will be one of the first European countries to substantially open up its telecommunications equipment and services market—a response to deregulation and market conditions, globalization, and telematics progress. The Dutch telecommunications equipment market is projected to reach nearly $800 million by 1990, while the European-wide market for equipment and services could exceed $50 billion.

Holland has ensured that its infrastructure — including PTT Nederland which will become a private company January 1 without regulatory responsibilities—will be able to handle not only today's basic speech, text and data exchanges, but tomorrow's needs for fast total digitalization, mobile and other new value-added services.

Here are some examples of Dutch developments in advanced telecommunications services that will be available to consumers, industry and governments.

ISDN Picture Phone—Since 1983, the Dutch have been helping to define the operational standards, compatible with both CCITT and CEPT, for a worldwide small band ISDN videophone terminal. This international effort is being coordinated by the PTT Dr. Neher Laboratories and foresees low-priced picture phones for office and home use in 1992. High-quality moving pictures accompanied by high-quality voice are transmitted over a 64kbit/second network. The bit rate is achieved by data compression techniques that eliminate redundant information using a hybrid method combining DPCM- and transform-coding. Encryption will ensure privacy. To enhance a possible videophone service, high quality videotext images can be transmitted with the same equipment.

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Teleports—Designed jointly by Rotterdam's municipal authorities and its business community, the teleport uses the International Transport Information System (INTIS) for the electronic exchange of standardized messages between shippers and suppliers of all modes of transportation. Shippers and freight forwarders already access the network to send shipping instructions to deep-sea carriers and liner agents. They, in turn, communicate electronically with container terminals. Both PCs and mainframes, equipped with a 3780 emulator and a V22bis modem, can access the network. Access by X.25 protocol will be available soon. Amsterdam is also developing a teleport.

Transportation Databases—A standard IBM SNA system with videotext is providing more than 1,500 subscribers throughout Europe with cost savings and real-time information about space availability, type of cargo handled, destinations, departure and arrival times for trucks, trains, ships and airplanes throughout Holland. Called Transpotel, this Dutch database service has expanded through franchising to the United Kingdom, Switzerland, Belgium, Austria, France, Germany and Scandinavia, and soon will extend to Italy and Denmark.

In addition, Holland is a major manufacturing location not only for N.V. Philips's data communications products, but also for Alcatel, N.V., which builds and markets its System 12 for small and medium-sized firms; for Swedish multinational L.M. Ericsson, which manufactures telephones for the Dutch PTT and other telecommunications equipment; for West German multinational Siemens, which produces data communications products; and for the AT&T/ Philips joint venture, which is building a new generation PBX.

Further, three technology universities—at Delft, Twente and Eindhoven—and more than 100 technical institutes along with the Netherlands Organization for Applied Scientific Research (TNO) and major software houses assist companies, regardless of location, with research and development from defining systems needs to designing networks to building prototypes or writing code.

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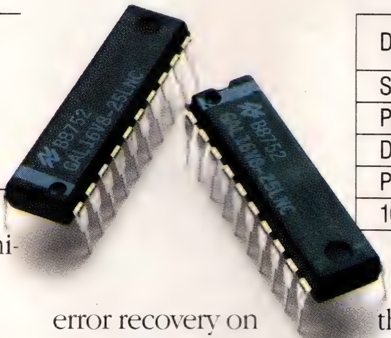

Device Type	ECL PAL	TTL PAL	EECMOS GAL
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Power	highest	high	low
Density	low	medium	high
Programmability	OTP	OTP	100%
100% Testability	no	no	yes

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Circle 55 on reader service card

partment at Hamburg-based Valvo, which is Philips' components-producing arm in Germany.

Jessi's status as a pan-European project did not always seem assured. Earlier this year, the project was clouded by disputes between Siemens and SGS-Thomson over the latter's participation [*Electronics,* April 28, 1988, p. 43]. Siemens apparently feared it would suffer in component markets if it had to share with SGS-Thomson the know-how gained in Mega, a joint Siemens-Philips project targeting a memory process.

"The whole affair was overblown," Weinerth insists. Given the magnitude of Jessi, "we all welcome Italian-French participation [in order] to share the cost." Indeed, intensive talks among Philips, Siemens and SGS-Thomson are underway. "I'm optimistic we'll reach an agreement soon," he says. Discussions are also being held with Plessey Ltd. of the UK.

It is not yet clear how SGS-Thomson and Plessey will participate in Jessi. A likely deal would be one in which each company in the group brings its expertise: Philips with static RAMs, Siemens with dynamic RAMs, SGS-Thomson with electrically programmable read-only memories, and Plessey with application-specific integrated circuits. "Such distribution of tasks would make sense," Weinerth says.

Whatever form Jessi will take, the project is getting moral backing from the Commission of the European Economic Community. The organization has indicated that it wants Jessi to be a pan-European project and members of the commission think that both producers and users of semiconductors should be involved in the project. Most likely there will be a link between Jessi's work and the work done under Esprit, the European Strategic Program for Research and Development in Information Technology.

Although Philips and Siemens are in favor of bringing more European firms into Jessi, they don't want a continent-wide program if it means postponing Jessi's launch. If potential partners drag their feet in current talks for tactical reasons, "we'll go ahead with the project as planned," Weinerth says. "In view of the Far Eastern competition, we cannot afford a delay."

To accomplish its mission, Jessi's architecture has been based on four pillars: technology, applications, equipment and materials, and basic research. The planning team is lining up semiconductor firms, equipment makers, software houses, institutes and university groups to work in these four areas.

The structure differentiates Jessi from Sematech, the U. S. semiconductor research cooperative with which the pan-European effort is often compared. Initially, it appeared that the two would be organized along similar lines, but it turned out that there are differences. At first it seemed that Sematech and Jessi would be constructed along similar lines, Weinerth recalls. But at some point the U. S. project changed its goal and focused on manufacturing technology only. "While ours is a four-pronged approach, Sematech puts the emphasis squarely on manufacturing technology," Weinerth says. He adds jokingly that Sematech looks like a declaration of war against Japan, whereas Jessi is less belligerent with its catch-up strategy.

Weinerth is optimistic that Siemens and SGS-Thomson will soon settle their dispute.

Weinerth is well aware of the challenges that Jessi poses. The technological challenges are symbolized by the tip of an 8-in. silicon ingot on his desk. "In working with wafers made from such size ingots, our technologists have a big job ahead of them," he says.

More European firms may be brought in, but only if Jessi's launch is not delayed

Just as challenging are the jobs that must be completed before Jessi is able to get on course. During the months ahead, important decisions must be hammered out. This fall, talks with the user side will begin, Weinerth says, "and it may prove not all that easy to sort out what's needed in the way of tools and design equipment." Fourteen firms, from large ones such as Nixdorf Computer AG and the Robert Bosch group to small outfits in Belgium, are supporting Jessi's thrust into the applications environment.

Weinerth sees a way to avoid the political minefield that picking a central site for Jessi would turn out to be. Earlier this year, German politicians' tempers flared over where to put headquarters—in technologically exciting Bavaria, which is in Siemens's backyard, or in job-hungry, economically depressed regions in Northern Germany, which are closer to Philips's home. "Once the French and Italians come in, we may decide on decentralized control, with each firm overseeing Jessi operations from its own premises," Weinerth predicts.

FINDING PERSONNEL. What may turn out to be a problem, however, is finding enough personnel to staff Jessi. "With European universities and engineering schools delivering excellent people, it's not a question of quality," Weinerth says, "it's a question of sufficient quantity on a high-quality level." In the end, Jessi may have designers from all parts of the world including the U. S. and the Far East.

Another challenge is to convince the public of the need for funding another microelectronics venture—after all, to many outside the technological community Esprit would seem to be enough—when many believe there are more pressing social problems. Furthermore, governments must be persuaded to match the industry's expenditures.

Although often compared to Philips-Siemens' Mega project, Jessi targets a new, broadly applicable technology generation and the required infrastructure while Mega, scheduled to end next year, targeted a memory process and two products. They were the 4-Mbit dynamic RAM by the German firm and the equally complex 1-Mbit static RAM by the Dutch company. The Philips and Siemens RAMs will be made in volume next year.

Jessi's origins trace back to 1983-1984 when the Japanese said they would have a 300-Mbit memory by the mid-1990s. As alarmed as industry leaders and govenemnt officials in the U. S. were, those in Europe began considering an appropriate response. Their answer turned out to be Eureka 127, an official project of the European Research Coordination Agency, or Jessi.

The project's initial supporters were experts that included representatives from Philips, Siemens, a West German research organization called the Fraunhofer Institute, and a Dutch research organization called STW. They pursued the original initiative of the national submicron consortiums in France, West Germany, and the Netherlands.

With its technological ducks lining up nicely, and its rich historical context, Jessi seems well on its way toward an impressive beginning—provided Europe's politicians can resolve their differences quickly. "If we can come to terms with the politicians," says Weinerth, "and I think we will before the end of this year, Jessi will take off in early 1989 as planned." *–John Gosch*

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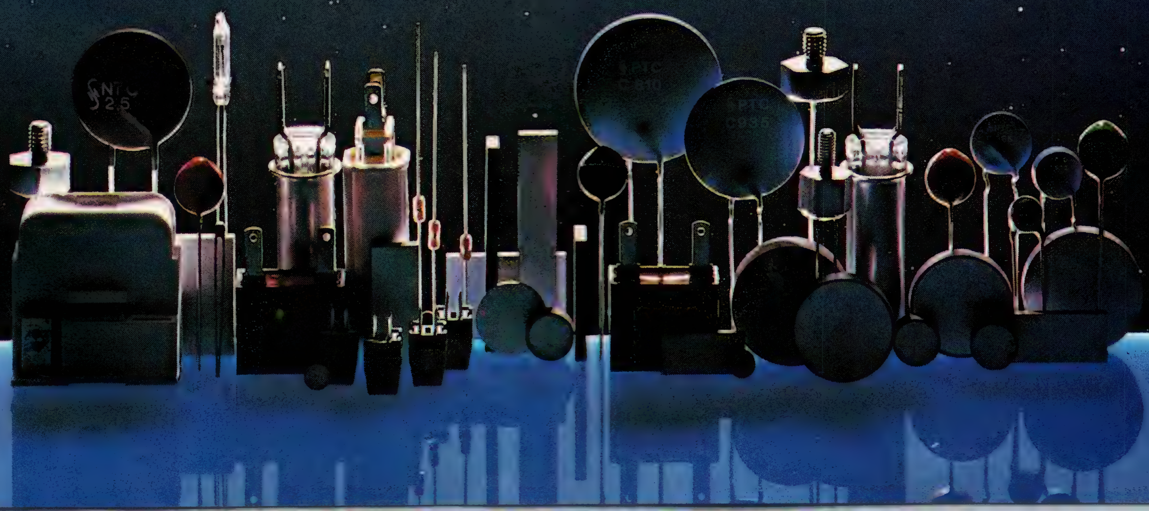

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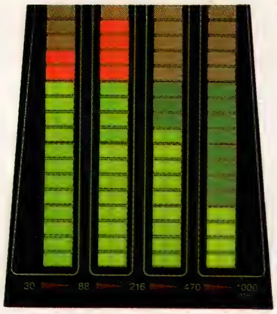

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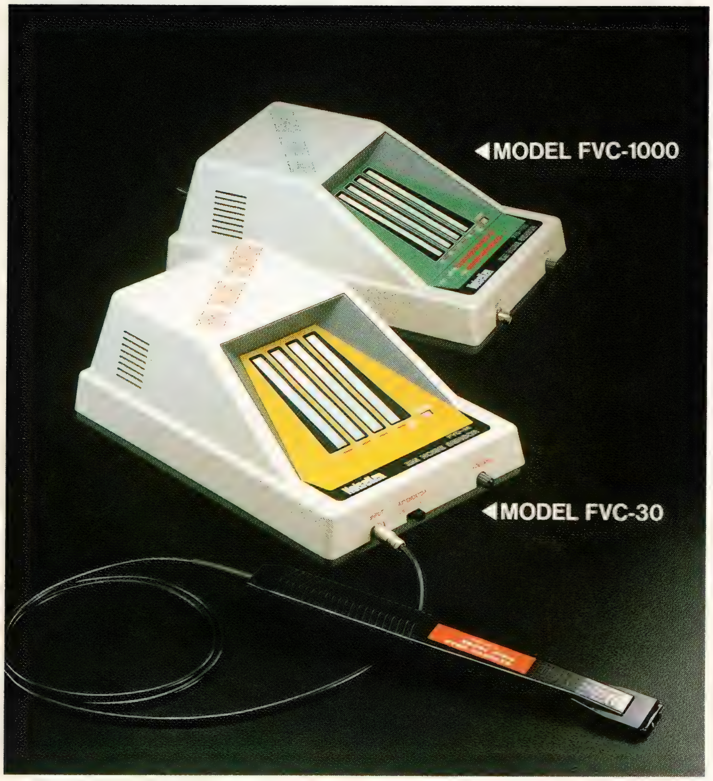

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Microprocessor-based Ibis-1 offers real-time performance with fast application development

KAMIFUKUOKA, JAPAN

A new microprocessor-based exchange that runs under two operating systems is built for integrated services digital networks and will power Japan's initial foray into international ISDN service.

The product of a joint venture between NEC Corp. and Kokusai Denshin Denwa Co., the exchange is called Ibis-1, which is short for Integrated Backbone Architecture for ISDN Systems. To solve the real-time, multitasking challenge inherent in telecommunications, Ibis-1 teams an Itron real-time operating-system kernel with Unix. The combination of a multiple-microprocessor architecture, based on NEC's V60 and V70 devices, plus Unix give the exchange's users a powerful tool for developing Ibis-1 applications.

Ibis-1 will serve all types of ISDN systems, says Katsuyuki Yamazaki, a scientist at the Telecommunication Network Laboratory in the Kamifukuoka Research & Development Laboratories of KDD, which is Japan's traditional overseas telecommunications carrier. It will handle the Consultative Committee on International Telephone and Telecommunications' No. 7 signaling transfer-point systems, large-scale international transit switches, and telecommunication network systems.

APRIL START. Limited ISDN service between Japan, the U. S., and the UK is scheduled to start next April. Initially, service will be available only to subscribers with dedicated lines to KDD, but it will soon be interoperable with ISDN and other services from Nippon Telegraph and Telephone Corp.

In the Ibis-1 exchange, the Itron operating system controls the actual communication channel switching, while Unix supplies the user interface for operation and maintenance. Itron was selected for its ability to handle multiple tasks in real time, a necessity in communications switches. In the Unix environment, programming, including applications and system support, is done in the C language. Although implementing Unix was not difficult, engineers had to overcome several inherent problems Unix had in assimilating Itron data to build a relational data base.

All development is done in C under Unix, using cross-development software if necessary. In the past, software has often been written in Chill, an internationally standardized language for communications switches. Because Chill is a single-purpose language, users were required to provide their own training and applications development tools.

Unix's excellent file system and its support of C open the door to a broad range of support tools. In the hands of the growing number of engineers skilled in their use, these tools can keep costs low for applications development.

While most previous switches have used special-purpose hardware, Ibis-1, by contrast, uses general-purpose devices: a large number of VLSI microprocessors in a fully distributed architecture. Initial versions are being built with NEC's 32-bit address/16-bit data bus V60 processors, but later units will feature the full 32-bit V70 that has a 32-bit data bus.

The Ibis-1 exchange can be used in a broad range of telecommunications networks including local switch, transit switch (also called tandem exchanges by some telephone engineers), transit-local switch, and private automatic branch exchange. The initial Ibis-series design is for a small ISDN switching system.

In each switching unit, the Ibis-1 offers a capacity of 4,096 64-Kbit/s channels for conventional speech-path networks. In the ISDN mode, it handles 1,440 lines for the basic-rate interface and 120 lines of the primary-rate interface. Each basic-rate interface line carries two data channels and one signaling channel, a configuration commonly referred to as 2B+D. For ISDN's primary-rate interface, both the European 30B+D configuration and the U. S./Japan 23B+D configurations are implemented. The transit trunk has 1,440 channels, each capable of 64 Kbit/s transmission (see table).

The basic interface implements an echo-canceLler operation rather than the ping-pong scheme favored by some Japanese integrated circuit manufacturers. Although the 30B+D primary interface adopted by European countries is not used by common carriers in Japan, it is included because the Ibis-1 is targeting an export PABX market.

For packet switching, the system uses an out-of-band control procedure based on a frame-switching method. This new packet mode has not yet been standardized by the CCITT but has been discussed as a third step in the ISDN packet evolution scenario, and could be adopted in the next study period, which starts in 1989. In addition to ISDN communications, the switch is equipped to handle all previous digital modes including public-switched telephone networks, packet-switched public data networks, circuit-switched public data networks, and telex networks.

NO STANDARDS YET. To handle this diverse collection of networks, the subrate, or slower, data can be carried on both the B and D channels for applications such as Telex, low-speed digital data such as personal computer communications, and digitized voice messages at rates lower than 64 kb/s. Subrate speeds have not yet been adopted by the standard-makers at the CCITT, so standardization still could be several years away. However, su-

IBIS-1 TARGETS MID-RANGE ISDN

CAPACITY	Speech-path network		4096 channels (64 Kbits/s/channel)
	ISDN Interface	Basic rate	1440 lines (2B+D)/line
		Primary rate	120 lines (30 or 23B+D)/line
	Transit trunk		1440 channels (64 Kbits/s/channel)
ARCHITECTURE	Circuit switching		Non-block switching of subrate for 32-, 16-, 8 Kbits/s
	Packet switching		Frame switching method based on the out-of-band packet procedure

brate capability could be used in PABX applications in the meantime.

The exchange is configured of up to eight switching units with each consisting of modules interconnected by a 32-Mbit/s IEEE 802.2 optical local-area network. Each module consists of one or more microprocessors and associated components. The actual main switch, though, is hardware. Also connected to the optical bus are an operation and maintenance subsystem and a service management subsystem that use the same microprocessors as the switching-unit modules. In addition, because the system bus is a standard local area network, other functions including artificial intelligence could be added. *– Charles L. Cohen*

MEMORIES

INTERMETALL SEES A FUTURE IN FRAMS

FREIBURG, WEST GERMANY

Intermetall GmbH is jumping on the bandwagon of a newly resurgent technology—ferroelectric random-access memories—and is hoping to ride it to a marketing edge in consumer electronics. But rather than attack entrenched memory technologies head-on, the Freiburg company will integrate the high-density, nonvolatile FRAMs into existing chips, particularly digital signal processors. First parts are expected in mid-1989.

The production equipment that Intermetall, the lead house of the ITT Semiconductors Group, is about to install will give it the European lead in high-volume FRAM production processes. Readying these processes—and solving some compatibility problems—are key to the firm's 0.8-μm integrated-circuit program, for which it has earmarked money "in the order of tens of millions of dollars," says company spokesman Reinhard Preuss.

At present, a pilot FRAM pilot line is running in parallel with one for 1.5-μm CMOS devices, and an 0.8-μm pilot line will be in place by the end of 1989. The quick installation pace is remarkable, considering that Intermetall bought into the FRAM business just this summer, through a six-year codevelopment and licensing pact with Ramtron Corp. of Colorado Springs, Colo. Ramtron is one of two U. S. startups (the other is Krysalis Corp., Albuquerque, N. M.) to revitalize ferroelectric technology after it was written off as dead 15 years ago [*Electronics,* Feb. 4, 1988, p. 32].

CROSS-DEAL. As part of the agreement, Intermetall will pay royalties on the FRAM-based parts it sells. Also, Ramtron may acquire the FRAM production processes from Intermetall.

As inexpensive to fabricate as dynamic RAMs, FRAMs boast the nonvolatility of electrically erasable programmable read-only memories—they store information even under no-power conditions. Moreover, they are as fast as static RAMs and can reach the high density of DRAMs. "These are arguments enough for us to turn to FRAMs," says Horst F. Jenisch, Intermetall's contracts director, who negotiated the deal with Ramtron.

Integrated into a DSP, the FRAM can raise the processor's memory capacity more than ten-fold, to 250 Kbits and more. High-memory-content DSPs are in demand for audio and video signal processing, two applications that Intermetall is already targeting with its Digit 2000 Digital TV circuits. These popular chips will turn up in some seven million TV sets manufactured worldwide this year alone, or more than 10% of all color models. "With FRAMs on these chips, not only should we keep but also expand our share of the market for such circuits," Jenisch says. Indeed, because FRAMs are inexpensive to produce, the souped-up digital TV chips offering higher performance at virtually the same price may well attract new customers.

The DSP line is only one of the areas that has kept Intermetall a profit-maker over the years, often in the double-digit range. Key to the company's success is its commitment to producing devices the market wants at prices competitive with Far Eastern parts. And it has a long-standing strategy of buying, rather than developing, technology, using money that might otherwise have gone into research for process development, concept engineering, circuit design, and customer support. The Ramtron deal is just the latest example of this philosophy.

"Technology itself is only a means to an end," Jenisch declares. "Most customers are not looking for the latest technology in a device. What they want is a good price/performance ratio, regardless of what makes that possible."

But before the company can prove its point with FRAM-equipped DSPs, "we still have a few production problems to solve," says Peter McAdam, the British-born leader of Intermetall's Process Development Group. The main one is achieving compatibility betwen processes for the semiconductor materials and the FRAM's lead-zirconate-titanate (PZT) compound, a newly developed material that is a major cause for the current excitement about ferroelectric technology. Until PZT, FRAMs were merely a laboratory curiosity that stubbornly resisted mass-fabrication attempts.

For starters, the high-temperature, plasma, and wet-chemical cleaning processes must be compatible. Also, the FRAM's electrode material must lend itself to convenient deposition and must be easily etchable. In no way should the material and the processes influence ferroelectric phenomena.

Intermetall will handle development incrementally. At present the FRAM pilot line is running in parallel with that of 1.5-μm CMOS devices but the company is in the process of integrating them. In addition, by the middle of next year, when the first FRAM-equipped DSPs are available, the 1.5-μm process will have been scaled down to 1.2-μm. Finally, by the end of 1989, the company will be on line with its 0.8-μm process, with FRAMs integrated into it. *–John Gosch*

EPROMs

NEC'S 4-MBIT EPROM LEADS DENSITY RACE

KAWASAKI, JAPAN

Memory-hungry applications in office and factory automation will be able to take a big step up in density—and garner all the concomitant advantages—with NEC Corp.'s 4-Mbit erasable programmable read-only memory.

Fabricated in 1-μm CMOS, the μPD27C4001DZ offers access times as fast as 120 ns to satisfy the demands of such machines as laser printers (which also benefit from the 4-Mbit density, especially for Japanese-character kanji fonts), factory-automation equipment such as numerical-control circuits, and games. NEC engineers will describe the chip at the European Solid State Circuits Conference Sept. 21. Although both Tokyo's Toshiba Corp. and Intel Corp. of Santa Clara, Calif., have delivered papers on similar devices at earlier conferences, no other company besides NEC has yet introduced a product.

NEC is ready to deliver samples of the 512 K-word by 8-bit chip now. The 120-ns version is priced at $115, and slower devices with access times of 170 and 200 ns are also available at the same price. Production will start next January at a rate of 100,000 units a month.

The EPROM is sealed in a 32-pin ceramic dual in-line package with a large window (photo p. 56F) and has a standard Jedec pinout assignment. As a follow-up product, NEC engineers are already working on a one-time programmable

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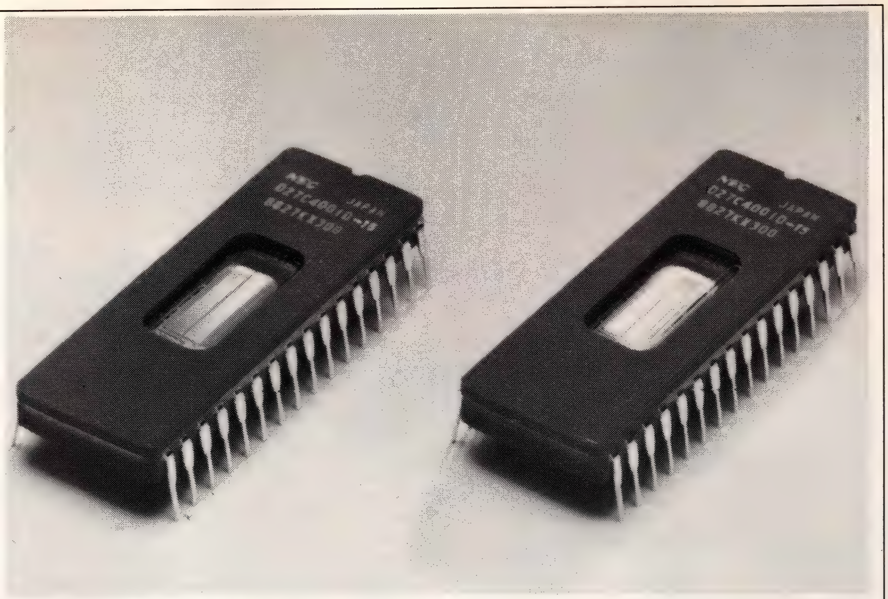
PHILIPS

version. Both devices will be compatible with the Kawasaki company's mask-programmable μPD23C4001E, which is already on the market.

The circuit boasts cell sizes of a mere 3 by 3 μm, and the entire design is fabricated on a 5.48-by-14.79-mm chip. The peripheral design features polysilicon wiring, an independent layer of silicide wiring, and a layer of aluminum wiring. According to NEC engineers, the layer of silicide wiring made fine-pattern fabrication simpler than using a layer of aluminum.

Excluding overhead, intelligent programming allows the entire device to be programmed in less than 60 seconds by using 100-ns pulses. Programming voltage is 12.5 V. Although present day 1- and 2-Mbit devices permit page programming, the μPD23C4001E offers only byte programming. And the device requires 30 mA maximum at +5 V during operation and 100 mA maximum during standby operation. *–Charles L. Cohen*



NEC's EPROM comes in a 32-pin ceramic dual in-line package with a large window and has a standard Jedec pinout configuration. Three speed versions are available.

ARTIFICIAL INTELLIGENCE

THIS TRANSLATOR EARNS B.A. IN ENGLISH

MUNICH, WEST GERMANY

After a decade in development, an artificial-intelligence-based natural language translator that works on a sentence at a time—using contextual as well as grammatical techniques—has been unveiled by Siemens AG. Dubbed Metal, for Machine Evaluation and Translation of Natural Language, the system goes beyond the cumbersome word-by-word translation method of earlier approaches. Siemens claims that Metal is the first translator of its type to be functional.

Metal translates German to English at a rate of about one word per second and delivers productivity gains on the order of 70% in applications such as translating user manuals. The system works best for technical writing, and attains accuracy so high that little post-editing by a human translator is required, Siemens says.

Written in Lisp and running on a work station manufactured by Symbolics Inc., Cambridge, Mass., Metal is available in an English-German version. The $135,000 price includes a Siemens MX2, a Unix multiuser system with four display-based work stations. It will soon be offered for French, Spanish, and Dutch pairings.

QUALITY WORK. Translation technology experts call Metal's quality "the highest that's possible with machine systems today," says Thomas Schneider, manager of the department of natural language processing in Siemens' communication and information systems division in Munich.

Siemens has also documented productivity gains. In a pilot installation at the public relations firm Compulex, Metal has cut the cost of text translations by 40% and the time to handle them by 70% compared with non-machine methods, reports Yvonne Attiyate, head of the Zurich, Switzerland, company.

The market for machine translation is already enormous. In 1986, more than 100 million pages of text were translated by hand in western Europe at a cost of $25 billion, according to Siemens. Growth is expected to continue at 15% a year.

Export-oriented companies are particularly feeling the pinch as the customers importing their products demand high-quality, full documentation in their native tongue. While a skilled person can handle 1,000 pages a year, Metal, on average, takes one second to translate a word. At that rate, the system handles about 200 pages of text (with tables, diagrams and other graphics) in an eight-hour day.

The Siemens system analyzes in complete sentences, not word-by-word

Besides industrial applications such as translating operating instructions, parts lists, catalogues, brochures and contract bids, the system will find uses in administration, specifically at world or super-regional organizations such as the United Nations and agencies of the European Economic Community. The 12 EC member countries use nine languages—Danish, Dutch, English, French, German, Greek, Italian, Portuguese and Spanish—which thus makes for 72 possible source and target language pairs.

Thus with its home in industry and administration, Metal is not intended for translating, say, a Shakespeare play into German or a Goethe poem into English, that is, for literary works where a word's nuances are crucial. Rather, it is for technical texts where words generally have a specific meaning.

Unlike other machine translation systems, Metal analyzes complete sentences. Each word is analyzed from a lexical point of view—in terms of ways it can be interpreted. The system then applies grammar rules and interprets all sentence elements until it has defined their functional relationships to one another. The elements are grouped into sentence parts such as a noun phrase, a verb phrase, and the like. A comparison of the many possible sentence structures is made until the most plausible one spanning the complete sentence is found.

For sentence analysis, Metal uses recursive grammar rules as well as a lexicon with information in coded form. The lexicon consists of modules whose terms are related to a specific field. For example, the German word *Fehler* translates to "error" in software engineering, "fault" in the computer hardware field, "defect" in automotive engineering, and "mistake" in ordinary language. This specific-module structure ensures that for each type of text the appropriate word translation is found.

The Metal lexicon modules are organized in a hierarchy. At the top are function words such as conjunctions, articles, and prepositions. Below that is a general

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Circle 302 on reader service card

vocabulary module covering everyday nontechnical words.

Next comes a common technical vocabulary containing words such as cable or telephone. Application-specific modules are defined by the human translator. For example, a "data processing" module may be subdivided into fields such as software, hardware, and so forth. The human translator also has the option of defining device-specific modules.

TARGET COUNTRY. Translation accuracy can be improved by defining the job in terms of a target country. Spanish in South America, for instance, is different form Spanish in Spain. And Spanish in Argentina is different from Spanish in New York. So translating the word "computer" into Castilian Spanish would produce "ordenador." A text targeted for Columbia would use the word "computadora."

To make Metal universally applicable, Siemens has a group in Belgium for developing the software for Dutch-to-French and French-to-Dutch translations, as well as a group in Spain for working on other language pairs and peculiarities of speech. There is also a 10-person group at the University of Texas in Austin, Texas, where American-English is analyzed.

Now capable of handling German/English translations, Metal will soon be offered for French, Spanish, Dutch and other language pairs.

Siemens' relations with the university date back to the late 1970s when the company's translation needs skyrocketed. Fully documenting its digital switch, for example, took some 100,000 pages. Siemens entered a cooperative deal with the university's Linguistic Research Center, which had many years of knowhow in computational linguistics. The Metal system uses approaches originally developed at the University of Texas.

Metal runs on a Symbolics work station, but for text processing and system management, the Siemens MX2, a Unix multiuser system with four display-based work stations, is added. Text can be inputed from a floppy disk, an optical character reader, or a keyboard. Any human translator can operate and manage the system after a brief introduction, so training costs are not high. The system automatically adheres to the original text format such as paragraph indications, indentations, tables, and flow diagrams, and delivers the translated output in the same format. *–John* Gosch

CELLULAR SYSTEMS

EUROPE, UK CATCH MOBILE-PHONE FEVER

LONDON

Skeptics who have long maintained that Europeans in general and the British in particular are not interested in gadgets are being proved wrong. It almost seems that the whole of European technological effort at the moment is concentrated on a most useful gadget: mobile communications. Activity is rising to a fever pitch in England, with the promise of a data network as well as new and less expensive services. There also are plans for a transatlantic paging system.

Some 400,000 customers have signed up with the nation's two cellular phone services in the past three years. Most of them are businesses that can afford the relatively high cost of nearly $1,000 to equip a car. But now field trials will start at the end of the year for yet another public mobile communications service—one that will offer phones for about $100. And the Commission of the European Communities has grabbed mobile communications services as a starting point for the unification of Europe.

First to commit itself to the pan-European standard was one of the two UK cellular operators, Vodafone Ltd., which placed $90 million orders with Ericsson Radio Systems AS of Sweden and Orbitel Ltd. in the UK. But Cellnet is the first to announce an opening date: using the pan-European standard, it will crank up operations on July 1, 1991.

Field trials will start by year's end on a new public service that will offer $100 phones

The company has signed letters of intent with Motorola Communications Group for equipment for network validation and testing, and is negotiating terms for a fully operational network. Validation will start in 1989. Industry insiders say Cellnet has earmarked about $750 million for its digital network.

The upshot is that Motorola has announced that it is adding 500 people to its Stotfold, Bedfordshire, work force on the strength of the order. Don Burns, managing director of Motorola UK, says Motorola will manufacture "the bulk of the equipment" for the new UK system.

The new demand for cellular phone equipment also is leading to more jobs on another front. Sales in the UK of conventional analog cellular telephones are soaring, so Orbitel has had to start a double shift for the 160 employees at its Nottingham factory to meet increased demands placed on it by its prime customer, Vodafone. Orbitel, which is jointly owned by Plessey Co. plc and Racal Electronics plc, has also increased its investment in production machinery by approximately $900,000 and is now turning out equipment capable of providing the equivalent of 140 cellular voice channels each week.

Meanwhile, with most users still thinking of cellular telephones for voice com-

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Circle 306 on reader service card

munications, ICL Ltd. has committed itself to full data communications. It is so eager to get started that it is prepared to use its own money to fill some of the gaps that still remain in the coverage provided by the Vodafone cellular telephone network.

The computer company wants to use the cellular network to provide instant data communications for each of its 450 field-service engineers, and is considering installing its own base stations in areas not yet covered, but where it has major computers, in order to get full national coverage.

Also on the way is equipment that costs less. By the end of the year trials are scheduled for Ferranti Creditphone Ltd.'s PhoneZone. This will use $100 pocket-sized digital cordless telephone handsets—known generically as CT2 for second-generation cordless telephones—for what is called Europe as Telepoint services.

CORDLESS PAYPHONES. The phones will be personalized with a firmware user identification. It will be usable in public places within about 200 meters of strategically positioned base stations known as Telepoints. They will effectively provide cordless payphone service, since usage will be billed automatically against a user's account. The same phone will also be used as a standard cordless phone in its owner's home, or as an extension for a private automated branch exchange in his office.

Not only that, but the Commission of the European Communities, emboldened by its success at getting the fiercely isolationist PTTs—the government agencies that operate each nation's communications services—into accepting the idea of a pan-European cellular telephone service, is going further. The EEC has awarded a contract to a consortium of 22 European companies, led by Philips of the Netherlands, for an effort called the RACE Mobile Project. The deal is worth about $21 million, half coming from the EEC.

Telepoint services will use personalized phones with firmware user identification

The object is to make mobile communications available to all in a convenient form and at an affordable price. It is understood that the target price for the user terminals has been set at around $75, although the project is aimed only at "laying the foundations which will be built upon by telecommunications administrations, service companies, and equipment manufacturers" rather than manufacturing or supplying a new system.

It won't be easy. The researchers will have to figure out how to locate users anywhere in Europe, route calls through the networks, and accommodate all users within a limited band of radio frequencies.

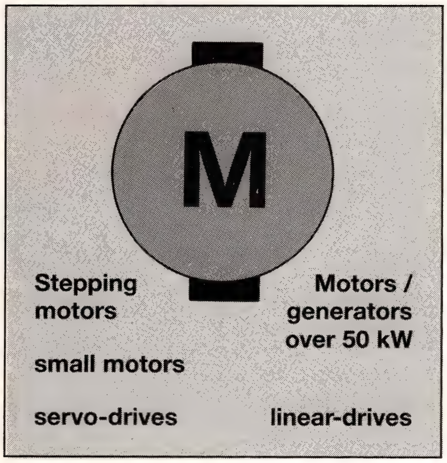
And finally, while European mobile communications firms are concentrating on pan-European projects in paging and cellular radio, British Telecom has its eyes set on even bigger markets. It intends to extend its radio-paging service to span the Atlantic Ocean and in 1989 it plans to launch a transatlantic paging service, based on its acquisition of U. S. paging company Metrocast.

Metrocast is a national paging service operator covering 82 cities in the U. S.. It uses a unique paging receiver able to operate on 14 different frequencies, and capable of scanning all of the major international paging frequencies.

British Telecom paid $16.9 million in cash for an 89% stake in the company. In addition, British Telecom will make $11 million available over a two-year period for system expansion. John Carrington, the company's director of mobile communications, says that after the introduction of transatlantic paging, the service has the potential for linking into the pan-European networks scheduled for operation in 1992.

–Peter Fletcher

RE-Permanent Magnets Advertisement



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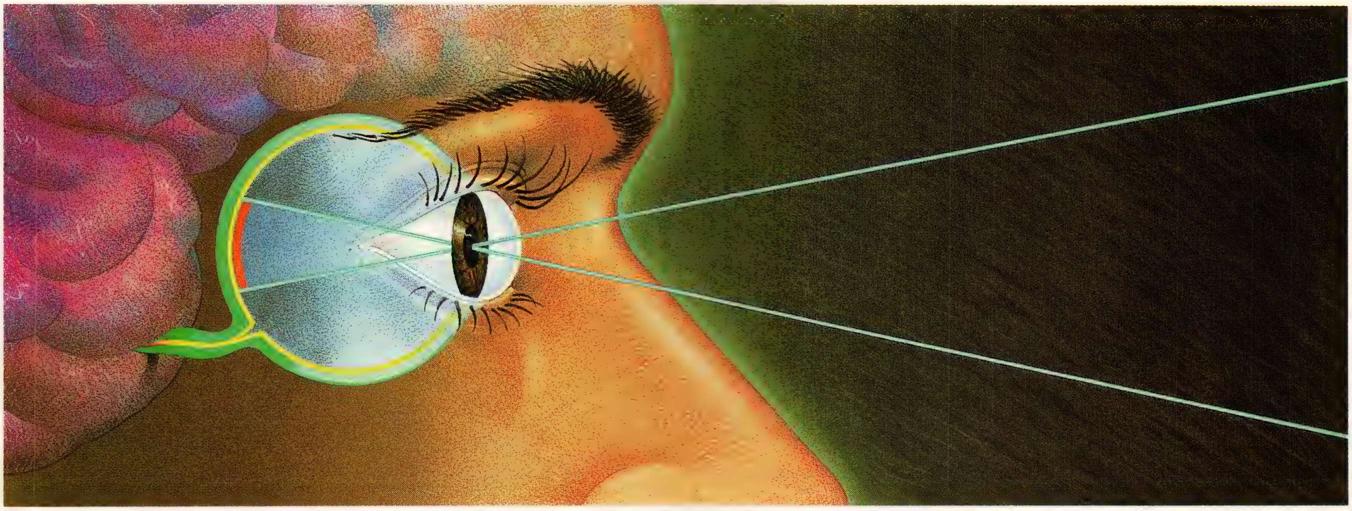
THE ANATOMY OF A FRAME TRANSFER SENSOR



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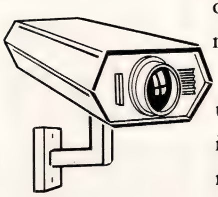

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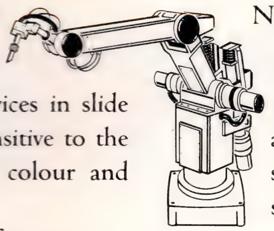

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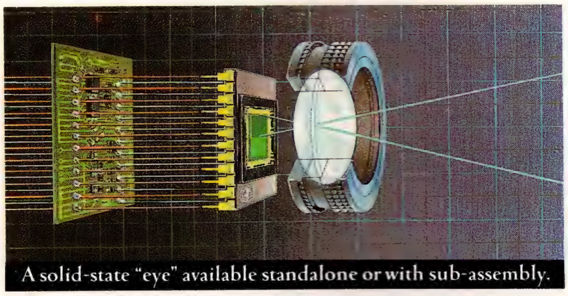

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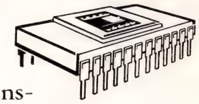

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SEPTEMBER 1988

WASHINGTON NEWSLETTER

WHAT WILL BECOME OF THE DOD'S X-RAY LITHOGRAPHY PROJECT?

The fate of the Pentagon's National X-Ray Lithography Program is up in the air. A spin-off from VHSIC, the Very High Speed Integrated Circuits program, the X-ray effort is supposed to help drive semiconductor processes below the 0.5-μm barrier and into the 0.25-μm region. But the fate of the program is in the hands of Congress, which is now struggling with President Reagan over the fiscal 1989 Defense Authorization and Appropriations bills. Now administered by the Defense Advanced Research Projects Agency, the X-ray venture received $15 million last year to fund work in X-ray mask generation at Perkin Elmer and Hampshire Instruments; development of advanced photo-resist technology at Spire Corp.; and advances in synchrotron design at Brookhaven National Laboratories. But with no money in the DOD's budget request for 1989, the program could be in danger. There's even some controversy over whether X-ray lithography will ever be a viable alternative to its optical counterpart. Recent advances in optical lithography seem to indicate that it may be viable for smaller geometries than many people thought, says David O. Patterson, Darpa's program manager for X-ray lithography. "But you can't wait until 1993 to start looking at X-ray," he says. "We want to demonstrate a quarter-micron capability by 1994." But without action and money now, that may become impossible. □

THE UNIVERSITY OF WISCONSIN SEEKS TO BUILD A SHARED SYNCHROTRON

The toughest part of making X-ray lithography into a widely used technology may not end up being development—it might be getting manufacturers access to synchrotrons, the electron storage rings needed to produce the X-rays. IBM Corp., which in July produced working N-MOS chips using X-ray techniques for the first time at Brookhaven National Laboratories, has ordered its own synchrotron. But most other companies have neither the capital nor the need for their own synchrotron. So the University of Wisconsin is trying to get funding from the Department of Energy and the Pentagon to establish a shared storage ring, with five beam lines set aside exclusively for X-ray lithography, says John D. Wiley, associate dean for research in the university's College of Engineering. Each line could then be outfitted with an aligner and other equipment needed for production—"whatever stuff they need to put on resist, expose it, and characterize the results," Wiley says—and the university would staff and support the facility. The facility might also offer a mask-replication service. "Most people are not familiar with this sort of light source," Wiley says. "They're going to need help, and we can provide it." □

THERE'S A NEW MAN AT THE HEAD OF THE VHSIC BANDWAGON

With only a year to go before concluding its long effort to inject advanced semiconductor technology into military systems, the Defense Department's Very High Speed Integrated Circuits Program is getting a new director. E. C. "Dick" Urban, who spent the last 16 years working in various Defense Department posts at the Navy, the Defense Logistics Agency, and the Defense Technology Analysis Office—and most recently as VHSIC's deputy director—becomes the new VHSIC and Electronic Devices chief this month. Urban replaces Egbert D. "Sonny" Maynard, the hard-driving taskmaster who shaped and guided the VHSIC program from its infancy and helped to force-feed the technology into high-profile military systems. After 24 years in government service, the last five as chairman of the VHSIC steering committee and the general manager for a range of leading-edge technology development programs, including the DOD's Ada and Mimic initiatives—Maynard says he's retiring from government service and his post as director of the Computer and Electronic Technology Office to seek a new challenge in industry. □

WASHINGTON NEWSLETTER

NOW THERE'S A TOOL THAT MAKES WRITING ADA SOFTWARE EASIER

Defense contractors have a new tool to boost programmer productivity in Ada, the software language required in all mission-critical Pentagon programs. Teamwork/Ada, from Cadre Technologies Inc., a Providence, R. I., computer-aided software engineering firm, draws on technology developed with Air Force funding—and licensed from General Electric Corp.—to allow programmers to write large-scale software programs using graphical notation instead of text. That notation can later be converted to validated Ada code automatically. Although the first version of the $3,500 package still requires some parts of the code to be done in text, Cadre promises a release by mid-1989 that will not only automate the graphics-to-code process entirely, but most importantly, will allow concurrent updates, so when users edit code in text form, the system will automatically generate corresponding changes in graphics—and vice-versa. ☐

DARPA TAKES FIRST STEPS TOWARD A 1,000-MIPS PROCESSOR

Pushing the computing envelope to the outermost limits, Encore Computer Corp. of Marlboro, Mass., is moving toward making a massively parallel computer that executes 1 billion instructions/s. Encore will demonstrate a prototype of its system, code-named Ultramax, in December. With $10.7 million from the Defense Advanced Research Projects Agency, Encore is trying to link two of its Multimax parallel processors with a two-board interconnect system. Encore is now debugging the interconnect boards and will soon begin linking the system's software with a derivative of Mach, a Unix-based operating system developed at Carnegie Mellon University, so that two Multimax systems can function as one. ☐

DOD'S COSTELLO ISSUES 'INDICTMENT' OF THE U.S. MANUFACTURING BASE . . .

When Robert Costello took over as under secretary of defense for acquisition one year ago, he promised an exhaustive study of acquisition policy and industrial competitiveness. Now his report is out, and Costello has issued a scathing indictment of U. S. manufacturers. "There is a pervasive problem with the quality and effectiveness of management in American manufacturing industries," Costello says. Worsening the problem, he says, is that the government can do almost nothing about it—these are business problems, he says. But Costello, who has been instrumental in a Defense Department-wide effort to streamline acquisition procedures, says the DOD can do its part by encouraging incentive contracts aimed at competitive cost reductions; limiting its intrusions into contractors' affairs; and pushing for tax changes that would encourage long-term investment in technology. ☐

. . . AS HE PROMISES FURTHER ACQUISITION REFORMS AT DOD

Contract managers must learn to look at the big picture when reviewing contract proposals and not just the bottom line, says Robert Costello, under secretary of defense for acquisition. The report on the industrial base wasn't just tough on contractors—it was hard on Pentagon acquisition managers too. Life-cycle cost analysis should be used to take into account the cost of maintaining a system as long as it is in the field, in addition to the cost of procurement, but the procedure is hardly used today, he says. The problem is that budget limitations encourage an over-emphasis on bottom-line price, making program managers reluctant to consider higher-priced options—even if they might save money in the long term. Costello says that although it would not be a cure-all, the DOD should experiment with life-cycle costing to cut weapon systems costs. ☐

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SEPTEMBER 1988

PACIFIC RIM TRENDS

NIPPON MINING EDGES INTO ELECTRONICS BY FORGING A DEAL WITH GOULD . . .

Add Nippon Mining Co. of Tokyo, and Gould Inc. of Rolling Meadows, Ill., to the list of partnerships between U. S. electronics companies and Japanese non-electronics firms. Each will have an equal share of Nippon Gould Computer Ltd., Tokyo, which will be capitalized at $460,000 and will sell Gould's NPL series minisupercomputers and Concept series superminicomputers. The NPL series, which has been sold in the U. S. since September 1987 has a peak execution rate of 40 million floating-point operations/s. The Concept series, which has been sold in both the U. S. and Japan since 1980, has an execution rate of 12.4 million instructions/s. Combined initial annual sales for the models is forecast at $7.7 million and is expected to increase to $38.5 million in five years. ☐

. . . WHILE SOFTWARE LURES FUJITSU INTO A PARTNERSHIP WITH SUN MICROSYSTEMS

Meanwhile, Fujitsu Ltd. and Sun Microsystems Inc. have agreed on a deal in which the U. S. firm will supply Fujitsu with Sun's complete line of work stations on a private label basis. Fujitsu figures the best way to offer its customers the rich library of more than 1,500 software products now available on Sun's platforms is to buy them from Sun rather than develop compatible systems. Sun's other vendors will continue to sell in Japan while Fujitsu will also sell in other markets including Australia. But Fujitsu, which produces the Sparc chips developed by Sun for its work stations, has not given up on its own work-station and software-development efforts. It will continue to offer its own Unix work stations—the G-200 series and the Σstation200. The G-200 series provides a high level of interoperability with the firm's M-series of mainframes. The Σstation200 is the designated platform for software development in the Japan's Sigma project to increase software productivity. ☐

CHIP MARKET'S REVIVAL SPURS NEC ONTO A DOMESTIC EXPANSION PATH . . .

The semiconductor market's recovery has pushed NEC Corp. into an expansion mode. The Tokyo-based firm will start construction in September on a VLSI plant in Hiroshima that it shelved five years ago because of the worldwide overcapacity in chips. The 36,000-m^2 plant, which may be the first to make 4-Mbit dynamic random-access memories and 1-Mbit static RAMs on a large scale, will start operation sometime after April 1990. NEC will spend $270 million to build and equip the plant, which will have a throughput of 30,000 6-in. wafers. That will amount to about 4 to 5 million 4-Mbit DRAMs a month—the largest capacity among Japanese semiconductor plants announced to date. The new plant will be operated by a new NEC subsidiary, Hiroshima NEC Co. ☐

. . . BUT SONY THINKS THE ROSIER PLANT SITES ARE IN THAILAND

Consumer electronics manufacturing on the southern Pacific Rim is now a big enough factor worldwide to prompt Sony Corp. to build a semiconductor manufacturing facility in a suburb of Bangkok, Thailand, just to serve that regional market. The 6,000-m^2 plant in the Bangkadi Industrial Park will go on line in October 1990 and is Sony's first overseas chip plant. Bipolar integrated circuits for compact disk players and other audio products are slated to be out by October 1990. The Tokyo-based company is so eager to add capacity, however, that in the interim it will lease space from AMD (Thailand) Ltd., a wholly-owned subsidiary of Advanced Micro Devices Inc., Sunnyvale, Calif. Production will start in April 1989 at a rate of 3 million bipolar ICs a month. When Sony's own plant in Bangkadi goes on line, production is expected to hit 10 million units. ☐

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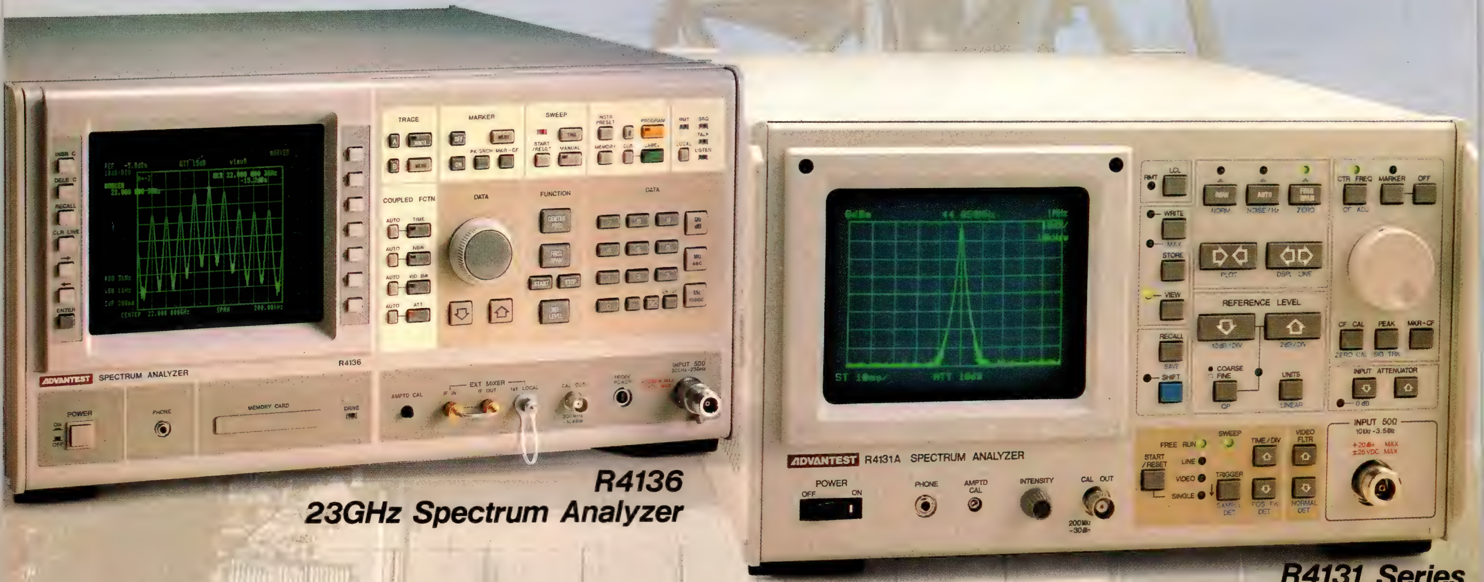
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EUROPE FORGES A UNIFIED FRONT ON WORLD TELECOM POLICY

Look for Europe's clout in setting international telecommunications standards and policies to take a quantum leap at the next regulatory conference. Meeting in Brussels, Belgium, last month, a dozen European telecommunication ministers pledged to vote as a block at the International World Administrative Telephone and Telegraph Conference to be held in Melbourne, Australia, in December. WATTC is expected to hammer out regulations for development of telecommunications on a global scale. The only block vote within the International Telecommunications Union—which is sponsoring the conference—has been the USSR, which has a vote for each of its 16 constituent republics. In a possible preview of their major thrusts in Melbourne, the ministers in Brussels emphasized the importance of high-definition television and advanced value-added services that meet both market and social needs. ☐

SIEMENS'S BIPOLAR RESEARCH HELPS KEEP GaAs AT BAY

Much to the chagrin of gallium-arsenide enthusiasts, silicon bipolar technology keeps getting faster. Its most recent advance comes from Munich-based Siemens AG, where researchers have developed an experimental static 16-to-1 frequency divider that runs at 15 GHz—almost half again as fast as the present record of 10.4 GHz reported by Nippon Telegraph and Telephone Corp. earlier this year. To attain the blinding speed, Siemens's researchers refined techniques developed at the company's Central Research Laboratory that delivered 8 GHz last year in an 8-to-1 frequency divider that used 2-µm silicon bipolar technology. The new device is based on 1-µm lithography, an improved doping profile, and optimized circuit design. Potential applications for the new device range from high-frequency measurement gear and fiber-optic transmission systems to satellite TV signal reception. ☐

THE BUNDESPOST GETS A 2-GIGABIT/S FIBER NETWORK TO DEVELOP . . .

A fiber-optic transmission system boasting laboratory speeds of 2.24 Gbits/s and carrying capacities equivalent to 30,000 telephone channels has been turned over to West Germany's Bundespost telecommunications authority for further research and possible commercial implementation. Developed by engineers at laboratories operated by Standard Elektrik Lorenz AG, a member of the French Alcatel N.V. telecommunications group, the system uses monomode fibers and a 1.5-µm wavelength. One of the most powerful fiber-optic systems developed as yet, it operates without repeaters for distances up to 115 km and boasts a bit-error rate of only 8×10^{-12}. The optical input power at the receiver is -30 dBm. Digital switching functions are handled by full-custom, fast silicon bipolar chips that were developed by Stuttgart-based Standard Electrik Lorenz. ☐

. . . AND FINDS IT HAS A NEW NETWORKING FOE NAMED SIEMENS

Siemens AG is joining the race to provide international public networking services to banks, insurance companies, airlines, and other industries that need fast, accurate communications with a decidedly international flavor. To chase that market, the Munich, West Germany-based electronics conglomerate and chip maker has formed a new subsidiary—Vascom GmbH—to compete with the Bundespost on its home turf. Vascom will offer customers the use of excess capacity on Siemens' internal corporate network, Siekom, which spreads around the globe into nearly 50 countries. Mainly operating in Europe, North America and Southeast Asia, Siekom uses Siemens's own switching equipment, and already includes some 80,000 terminals that communicate over leased lines and satellite links. ☐

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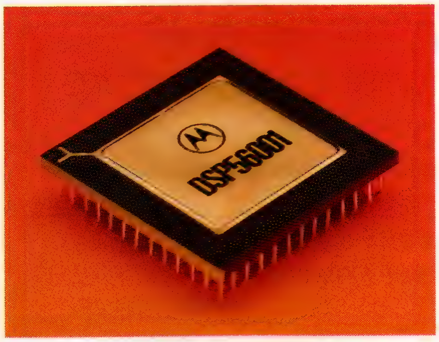

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GET SERIOUS ABOUT ANALOG ASICs!

Next-generation parts pump up performance and cut costs as pressure builds for design-tool breakthroughs

by Bernard C. Cole

Many systems houses are plenty serious already. And getting more so every day, as they see the performance and cost trade-offs improve in the latest generation of analog and mixed-mode analog/digital semicustom chips.

As their interest rises, they're putting heavy pressure on semiconductor companies to make the design of analog application-specific integrated circuits as easy as it is for digital ASICs, with all of the labor-saving computer-aided-design tools for layout, place and route, and simulation. They're also asking for the same fabrication alternatives: gate arrays and standard cells in addition to full custom.

What's making the industry get serious about analog and analog/digital ASICs is the shortage of experienced analog IC designers. Andrew Rappaport, president of Boston's Technology Research Group, estimates that the number of digital IC designers is about 20,000 worldwide and the number of systems designers is approaching 130,000. But the number of experienced analog designers is stagnant, he says, at a mere 2,000 or so.

DEMANDS. Furthermore, the demands being placed on both digital IC and system designers are mounting fast. Their employers want faster chips, denser chips, and shorter design cycles. And now they want analog and digital circuitry combined on the same IC.

The reason system manufacturers are lighting fires under their designers is simple: lower costs. "The way to reduce the overall cost of manufacture for a system is to reduce parts count and increase the level of integration," says Charles Gopin, vice president of marketing at MicroLinear Corp. of San Jose, Calif. An additional benefit, he says, is that "as a result overall reliability is increased, and maintenance and repair are decreased."

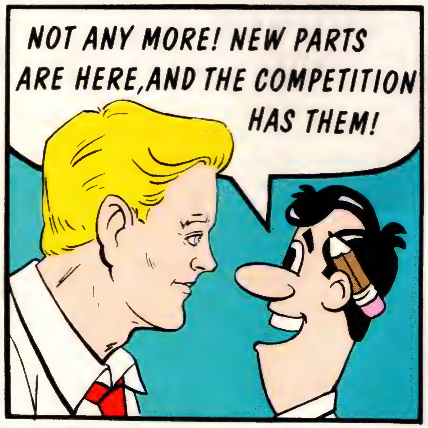
COME ON, FRED! THOSE THINGS ARE EXPENSIVE—AND THEIR PERFORMANCE STINKS!

But the stumbling block to further integration in many systems is the analog circuitry. "Side by side with VLSI-level microprocessors, memories, and custom and semicustom digital ASICs are dozens of discrete analog components," says Mike Berezuik, director of marketing for National Semiconductor Corp.'s ASIC division in Santa Clara, Calif. "The [systems houses] want to use the same types of tools and technologies to achieve the same benefits they have on the digital side."

Responding to this demand, linear-array vendors are pushing densities from 100 transistors or less to almost 1,000 transistors per chip, adding a few digital gates, and pushing speeds further into the gigahertz range. On the CMOS standard-cell side, digital vendors are adding 5-V analog cells to their families. For their part, traditional analog vendors such as Exar, MicroLinear, National Semiconductor, and Texas Instruments are coming into the market with high-voltage linear CMOS cell libraries.

But big technology challenges remain. One fundamental problem is the mismatch between what constitutes a good linear transistor and a good digital transistor. Linear characteristics degrade as device geometries push toward 1 μm, unless special processing and circuit-design techniques are brought into play. To get around this problem, manufacturers are adding biCMOS modules to their processes to allow the design of mixed-mode circuits with well-matched analog and digital sections.

A second major problem is simulation and modeling, a critical step in the design of any circuit. Where digital simulators need only describe the occurrence of a logic high or low at the output of a device, analog simulators must calculate voltages, currents, and temperatures associated with these states as well as the spectrum of voltages and currents the device develops in the transition from one state


NOT ANY MORE! NEW PARTS ARE HERE, AND THE COMPETITION HAS THEM!

to the other. And mixed-mode simulation, in which the circuit must be partitioned between digital and analog simulators, takes even more time and effort. How well the industry deals with these problems is crucial, says Derek Bay, director of design services at Analog Design Tools Inc., Sunnyvale, Calif. The solutions will determine how successful the analog and mixed-mode ASIC market will be, and how fast it will grow.

As in the digital world, both in ASICs and standard logic, the market for semicustom analog is segmented into two parts: one is aimed at higher performance and low to medium levels of integration, served mainly by bipolar arrays; the other, newer segment, is aimed at higher levels of integration and lower levels of performance, served mainly by CMOS standard-cell-based solutions.

The first segment is the more mature, and consists mainly of applications requiring real-time signal conditioning of the type needed in many military, industrial, and high-end data-storage applications. Targeted to displace standard linear bipolar building blocks such as op amps, regulators, timers, and comparators, this niche has been enjoying a 30% to 40% annual growth rate since the early 1980s. On the conservative side, Dataquest Inc. of San Jose, Calif., projects annual sales will grow from $158 million this year to $215 million in 1990 (see chart, p. 68). On the optimistic side is HTE Management Inc. of Scotts Valley, Calif., which expects sales of $220 million this year and $360 million in 1990. Although there has been a trend from all-analog toward mixed-mode bipolar arrays, the total chip area devoted to digital circuitry seldom exceeds 10%, because of process and performance limitations.

MIXING IT UP. Of more recent origin is the trend toward combining a significant amount of analog circuitry onto CMOS VLSI semicustom chips that are primarily digital in nature. Sales of analog-intensive CMOS gate-array and cell-based designs will more than quadruple by the start of the next decade, says Rappaport of the Technology Research Group; they will make up 3.5% of all cell-based designs in 1991, he says, compared with about 0.8% in 1985. He estimates that the percentage of all cell-based semicustom designs with analog functions will increase from 23% in 1982 to almost 40% in 1990. By that time, he projects, 45% of all cell-based semicustom designs will contain up to 25% of the transistors used for analog functions. Dataquest estimates that sales of mixed analog/digital CMOS semicustom ICs will double from about $750 million in 1985 to $1.5 billion in 1990.

REALLY?!! I WANT A FULL REPORT ON WHAT'S HITTING THE MARKET!

The earliest chips of the all-analog group, which were bipolar arrays, appeared on the scene back in the early 1970s, long before digital gate arrays. But only since the early 1980s have they seen significant growth, due to major improvements in performance and density.

Analog arrays have gone from a few hundred megahertz to npn-transistor toggle frequencies of 1 to 6 GHz and pnp-transistor rates of 0.9 to 2.5 GHz. The march continues toward the 10-to-15-GHz range. Densities have also increased from a few hundred active and passive components and transistors per chip to several thousand. At the same time, die size has been shrinking, moving the production-volume point at which analog arrays cease to be economically competitive with full-custom solutions from 50,000 to 250,000 units—and now, with the Flexar Delta arrays from Exar Corp., San Jose, Calif., to 1,000,000 units (see p. 83).

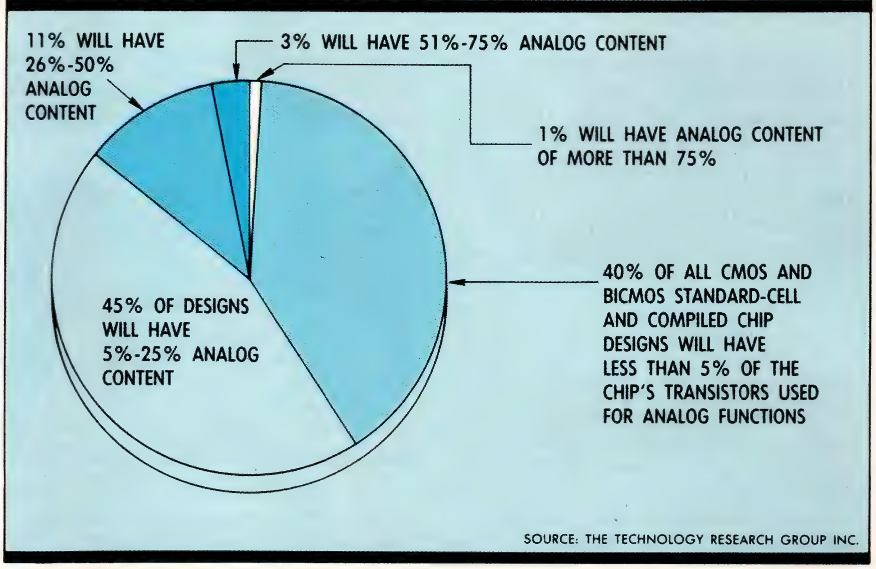
Leading the pack in terms of performance are AT&T, Plessey (see p. 78), SGS-Thomson Microelectronics, Tektronix, and VTC, all of which are targeting their analog arrays at applications requiring 1-GHz performance or better. AT&T Co.'s ALA200 features npn and pnp transistors

WHO HAS WHAT IN ANALOG ASICs

	CMOS	BiCMOS	Bipolar	Bipolar arrays	
	Standard cells				
Company	Analog/digital				Analog
Advanced Linear Devices	●				
Analog Devices		●			
AT&T	●				●
Cherry Semiconductor					●
Custom Arrays					●
Data Linear					●
Exar	●	●		●	●
Genum					●
Honeywell		●			
International Microelectric Products	●				
LSI Logic		●			
Microlinear	●	●		●	●
Motorola	●				
National Semiconductor	●		●		
NCR	●				
Plessey *				●	●
Raytheon					●
SGS/Thomson Microelectronics	●				
Sierra Semiconductor	●				
Silicon Systems	●			●	
Tektronix				●	●
Texas Instruments	●			●	
VTC	●	●	●	●	●
Universal Semiconductor				●	●

* Also sells CMOS analog/digital array products.

ANALOG INFILTRATION BY 1990



SOURCE: THE TECHNOLOGY RESEARCH GROUP INC.

with typical toggle frequencies of 4.0 and 2.5 GHz, respectively, whereas the J900 from VTC Inc., Minneapolis, features 6.5 and 1.0 GHz for npn and pnp, respectively. The family of QuickChip arrays from Tektronix Inc., Beaverton, Ore., features npn devices achieving 2.5 to 6.5 GHz and pnp performance at 20 to 40 MHz. SGS-Thomson of Agrate, Italy, offers the TSTJ04/J20, with 3.5-GHz npn and 40-MHz pnp transistors. Also addressing this market is DataLinear Corp. of Milpitas, Calif., which has applied dielectric isolation, instead of the traditional oxide- or junction-isolated techniques, to an analog array that features closely matched vertical pnp and npn transistors with a toggle rate of 1 GHz (see p. 72).

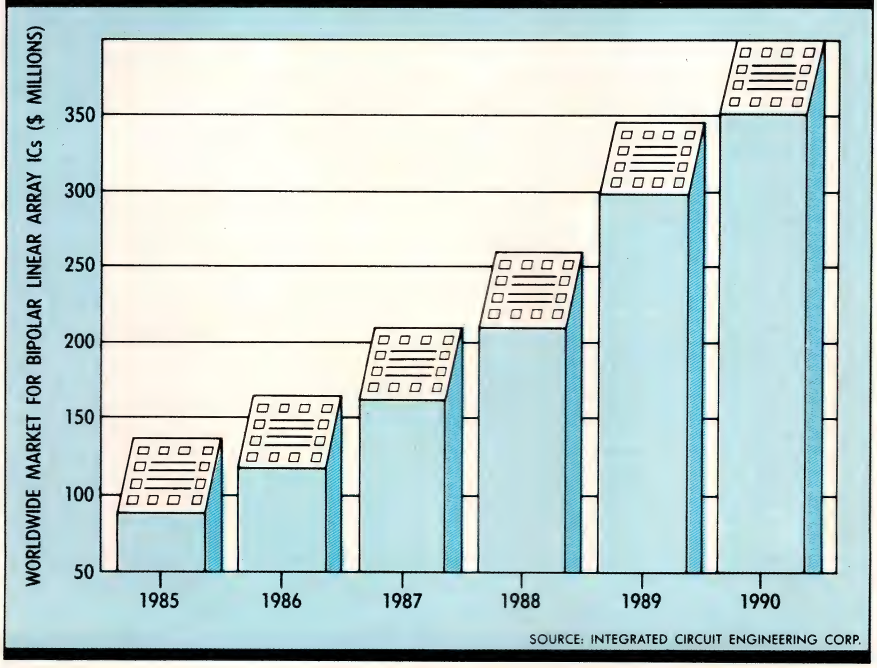
Trying to strike a balance between performance and density is MicroLinear, with its new FB3600 minitile-array family, a follow-on to its original FB300 array. Built using a 1-GHz, 12-V bipolar process, the FB3600 features a new architecture that combines up to 2,000 active components on a single die (see photo, p. 78). Its proprietary minitile architecture reduces by as much as 50% the die area required to implement analog circuit designs, says Gopin.

It also permits a unit-cost reduction of about 10% to 45% over an equivalent design built from discrete components, he adds. "With this array we have gone a long way toward eliminating the price premium associated with high-performance analog ASICs and made them economical in high-volume, 250,000-unit—or more—applications," he says. A key element in this design was the minimization of routing channels by using an analog variation of the channelless sea-of-gates architecture used in digital gate arrays to achieve higher packing densities, says Gopin.

Also pushing in this direction is Tektronix, which has developed what it calls a "standard tiles" approach, fabricated using a new oxide-isolated bipolar process with npn toggle frequencies in excess of 8 GHz. This new QuickTile series represents a compromise between the all-mask-layer full or semicustom approach and the one-mask-layer tile array, says Wink Gross, semicustom engineering manager. It uses "proto-arrays" that can be assembled with any standard graphics editor into an application-specific tile.

The tile array is then fabricated with an all-layer mask set, and customized by two-layers of metal interconnect. As with analog arrays, Gross says, the devices on the standard tiles are all precharacterized and modeled, simplifying circuit design. "Layout is easier than traditional all-custom, since the tiles snap together on a wiring grid," he says. "Thus the risk of layout-rule violation is low." Being evaluated and used internally, the QuickTile family is set for introduction in early 1989.

LINEAR ARRAYS SEE STEADY GROWTH



SOURCE: INTEGRATED CIRCUIT ENGINEERING CORP.

MORE DIGITAL. Bipolar array manufacturers like Exar, MicroLinear, and Silicon Systems are also feeling the pressure to incorporate more digital structures into their offerings and are slowly inching their way in to the mixed-mode world. Building on its earlier success with its Flexar Beta series of analog arrays, which use a general-purpose building block called the Twinstor, Exar is extending this concept to higher-performance, higher-density, and mixed analog/digital applications with its Flexar Delta Series. This family combines 1-GHz operation with the ability to mix analog and digital devices on a very silicon-efficient die.

Also looking to address this market segment, MicroLinear has come up with a modification of its new FB3600 family that incorporates digital circuitry as well. Designated the FB3635, the mixed-mode array has an analog section that can accommodate design complexities up to 8 op amps or 16 comparators. The digital section contains 130 2-ns emitter-coupled-logic NAND gates, allowing implementation of up to 42 latches or 21 flip-flops. In addition, a special set of input and output components allows interfacing to either TTL, CMOS, or ECL voltage levels off chip.

A newcomer to the fray is Silicon Systems Inc., Tustin, Calif., an ASIC supplier that has previously focused primarily on CMOS custom and semicustom analog/digital designs. Just introduced, the new bipo-

Simple as... *pushing a button*

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lar analog/digital array family, its 2-GHz MSA-6900 series, ranges in density from 1,458 to 7,470 components. There are up to 26 analog tiles and 24 digital tiles that can be implemented in either ECL or current-mode logic.

Like their digital cousins, linear and mixed-mode bipolar arrays can be brought to market in weeks or months, compared with the months to a year or so for full-custom designs. At the same time, though, they have the disadvantage of considerable silicon inefficiency. While recent introductions, such as Tektronix's "standard tiles" or Exar's Delta series, reduce the die-size differential between semicustom and custom from two or three times to under 50%, the gap is still there, says Tim Odell, vice president of the analog product group at National Semiconductor. "The fixed proportion of npn and pnp transistors on each array usually does not match the designer's needs," he says. "Nor does the density. Consequently many devices on the chip go unused." By contrast, for standard-cell designs, like handcrafted full-custom implementations using a complete set of masks, this problem does not exist, he says.

BIPOLAR CELLS. Looking to take advantage of the niche between bipolar analog and mixed-mode arrays and full-custom designs, a few companies have developed—or are investigating—bipolar standard-cell families. VTC has been on the market for a year or more with a bipolar standard-cell library, the VTC1000. Analog Devices Inc. and Honeywell Inc. have also developed bipolar standard-cell libraries, but they are limited as of now to internal use only. But National Semiconductor is joining VTC in this market with a bipolar standard-cell library, in an addition to its Custom Linear ASIC (Clasic) program. Fabricated using a proprietary 15-V linear bipolar process called LFAST [*Electronics*, Apr. 16, 1987, p. 67], it brings npn toggle frequencies of 2.5 GHz and pnp frequencies of up to 40 MHz to the standard-cell library, says Norman Miller, director of the Clasic program, includes 60 TTL- and ECL-based digital macrocells and an equivalent number of analog cells.

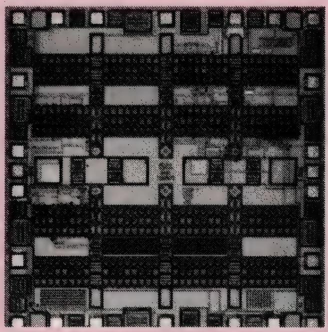
But no matter how attractive the relative stability and robustness of the bipolar analog and mixed-mode array markets, and the higher return on investment, the future of analog lies in CMOS, at least in the semicustom arena. According to Rappaport of the Technology Group, ASIC design starts for mixed-mode circuits since 1986 have increased three-fold, from about 2,000 or so to just over 6,000 in 1988. And in the next two to three years they are expected to catapult to about 30,000. In dollar sales, Dataquest estimates the market for mixed analog/digital CMOS semicustom designs exceeding $1.75 billion by 1991.

No wonder companies are jumping into the mainstream from both banks. On one

OXIDE ISOLATION BOOSTS ARRAY DENSITY

High-performance analog systems with one-tenth the component density of previous designs are now possible, thanks to a dielectrically isolated bipolar analog tile array from Sipex Corp.'s DataLinear division. Until now, equivalent performance could only be achieved with more costly and bulky hybrid or discrete components.

The Milpitas, Calif., company has scored an industry first by introducing its 440-transistor SP-1104 array, using a specially developed oxide with a breakdown voltage of 800 V. Other analog arrays rely on p-n junction isolation, which can significantly compromise high-frequency performance.


DataLinear's SP-1104 has an isolation-breakdown rating of 800 V.

The SP-1104 matches the best performance offered by discrete analog devices: high gain, with betas up to 200; high output current, up to 100 mA; and high-bandwidth, tightly matched bipolar transistors. Npn transistors are capable of toggle rates up to 1 GHz and pnp types have toggle rates of 600 MHz or more. The array can implement the design of analog circuits with bandwidths up to 30 MHz, gains to 120 dB, and offset voltages of less than 100 mV. And by using laser trimming, its on-chip resistors can be matched down to 0.01%.

Besides the radical reduction in component count, the array has another advantage, says William Dennehy, director of marketing at DataLinear. The full isolation of each transistor allows the use of conventional discrete-component design techniques like those used at the board level, he says, eliminating transistor-level problems. "Currently, with semicustom analog standard-cell or array alternatives, if systems designers want to integrate their high-performance discrete linear bipolar circuits, they must deal not only with the normal difficulties, but a whole range of transistor-level factors as well," Dennehy says.

The problem has been that most bipolar analog arrays use conventional junction-isolation techniques, which achieve isolation by a reverse-biased p-n junction between individual circuit elements and the common substrate. While this provides reasonable levels of isolation, the junction itself is a parasitic element that can degrade circuit performance. Also, such isolation techniques suffer from severe leakage currents associated with the reverse-biased junction, especially at high temperatures.

In DataLinear's dielectrically isolated array, the p-n junction has been replaced by a high-quality silicon dioxide dielectric layer with an 800-V breakdown rating, virtually eliminating these transistor-level problems. "For all practical purposes, the system designer defines and lays out the linear functions he needs in more or less the same way he would at the board level," says Dennehy. "The only parasitics are the island-to-island capacitances associated with the dielectric layer. When compared to those in a junction-isolated device, these are negligible; they have no voltage dependence."

The 143-by-140-mil SP-1104 contains a 4-by-4 matrix of tiles, each with 12 small-geometry npn transistors and 12 pnp transistors with collector currents ranging from 10 nA to 5 mA for use in either signal-path or bias-circuit applications. On the top and bottom of each tile is a clear area reserved for 36 user-defined thin-film nichrome resistors. Between the tiles are six buried zener diodes and six 5-pF capacitors, as well as 24 vertical, double-base-contact pnp and npn transistors. Collector currents range from 50 mA up to 20 mA, for use in driving internal nodes at high slew rates or for driving an output. Around the periphery and down the center of the device are eight large (8 to 18 pF) capacitors, 16 medium-current (100 nA to 30 mA) double-base, single-emitter, double-collector transistors, and 12 high-current (1 to 100 mA) double-base, triple-emitter, double-collector transistors.

MACROFUNCTIONS. Implemented as a family of predefined macrofunctions developed by the company, the array is symmetric about the two perpendicular center lines; elements are linked by two aluminum interconnect layers. The macrofunctions consist of voltage references, current references, precision op amps, transimpedance amplifiers, and comparators. Macrofunctions are usually configured to fit one or more tiles; but in many cases, Dennehy says, some macrofunctions use less than one tile.

Available with collector-emitter output voltages of 20 or 35 V, the SP-1104 is supported with a full set of Spice model parameters, which can be used on any of a number of industry-standard simulators such as P-Spice and H-Spice. A layout package, which runs on GDSII-compatible work stations, is also available. Nonrecurring engineering cost for the SP-1104 starts at about $20,000 and includes 25 prototypes. *—B. C. C.*

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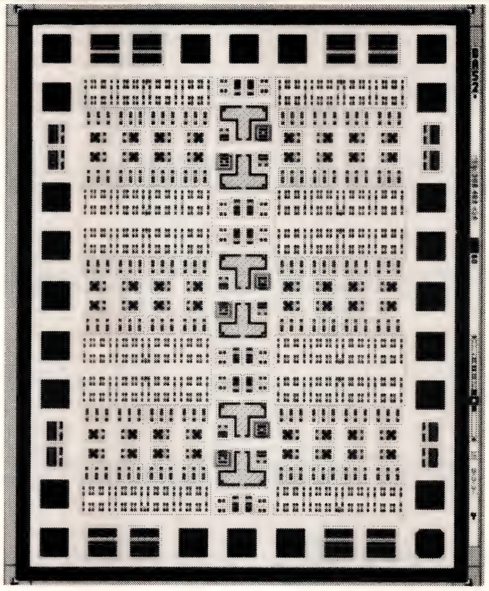
side are the traditional digital CMOS semicustom vendors, such as LSI Logic, Motorola, NCR, and VLSI Technology, which are offering 5-V-only analog cell additions to their existing digital libraries. On the other side are traditional analog houses such as Analog Devices and Advanced Linear Devices, plus linear semicustom firms such as Exar and MicroLinear, among others. They have developed higher-voltage (10- to 40-V) mixed-mode CMOS standard-cell offerings. In the middle are a select few companies with capabilities in both segments, among them International Microelectronic Products, National, Sierra Semiconductor, TI, and VTC. They have standard-cell offerings in both segments.

Indicative of the direction of 5-V-only mixed-mode standard-cell technology is the 1.2-μm 5-V p-well CMOS offering from International Microelectronic Products Inc. of San Jose, Calif. (see p. 82). This technology is at least one generation ahead of any other analog/digital CMOS-based standard cell currently available. Going in the other direction is Exar, with its N2000 2-μm, 20-V CMOS mixed-mode standard-cell family.

But a few companies perceive that at low densities, in particular, analog and mixed-mode arrays, with their single customization metalization layer, make as much sense in CMOS as they do in bipolar or digital CMOS, offering as they do a shorter time to market. Two companies that are moving aggressively into this niche are Plessey and Silicon Systems.



A 1-GHz bipolar minitile array from MicroLinear strikes a balance between performance and density.

Plessey Semiconductors Ltd., Swindon, UK, unveiled this month a family of eight mixed-mode arrays fabricated using a 3-μm, 18-V CMOS process. They range in density from 400 MOS FETs and 45 logic gates to 2,500 MOS FETs and 1,150 gates. Featuring internal toggle rates up to 50 MHz, the arrays have a structured architecture that allows the design of circuits using a comprehensive library of 50 digital and 20 analog macrocells. And set for release later this year is the MSA-6700 family from Silicon Systems. Built using a 3.6-μm, 12-V CMOS process, the array family will initially include three devices, ranging in density from 512 to 1,024 digital gates and from 10 to 32 analog tiles.

FOUR PROBLEMS. Despite the frenzied activity to date, it is clear that if the trend toward semicustom analog and mixed-mode ASICs is to continue, at least four fundamental problems must be solved. One is resolving the performance and transistor-size mismatch between analog and digital circuitry. Second, a way must be found to maintain good analog performance as device sizes are scaled down to accommodate digital VLSI densities. Third, as analog densities increase, more efficient simulation models need to be developed. And fourth, as the analog component of a mixed-mode design increases, more efficient and reliable ways of performing combined analog and digital simulation are needed.

To address the first two problems, a

PLESSEY'S HIGH-DENSITY BIPOLAR ARRAYS TOGGLE AT 4.5 GHz

Targeting high-performance analog applications in communications, computer peripherals, and control systems, Plessey Semiconductor Inc. is unleashing a bipolar analog array series that combines multigigahertz performance with unprecedented integration levels—up to 2,000 transistors on a single die.

The new family combines Plessey's innovative features with technologies from Ferranti Interdesign Inc., which the company's parent firm, Plessey Semiconductors Ltd. of Swindon, UK, acquired early this year. At the heart of the new circuits, contributing both to their flexibility and density, is Plessey's universal npn/pnp structure called the "monistor." The multipurpose transistor can be used as either an npn or pnp transistor, depending on how it is configured, with all the n- and p-type regions necessary. Also contributing to design flexibility is a repeated-cell symmetrical tile architecture that was developed at Ferranti.

The first devices in the new MF series will include five arrays ranging in density from 109 to 696 transistors with toggle frequencies up to 4.5 GHz. In addition to higher-density analog arrays, the company is developing arrays that will push performance higher on mixed analog/digital devices, says Richard Padovani, analog application-specific IC product manager in Scotts Valley, Calif. The mixed-mode arrays will incorporate up to 215 emitter-coupled-logic gates, the equivalent of 1,090 npn transistors, in the largest array.

The MF series supports a range of linear applications from very fast linear signal processing to ultra-low-current low-frequency circuits. The arrays are therefore ideal for communications applications such as very high-frequency modems, mobile telephones, video equipment, data-acquisition hardware, low-noise amplifiers, and servo demodulators, says Padovani.

A universal npn/pnp structure contributes to flexibility and density

Circuit performance ranges from video amplifiers with bandwidths of several hundred megahertz all the way to comparators with 1- to 2-ns delay time, or ultra-low-power linear circuits of more modest bandwidths.

Introduction of the new series was delayed about six months due to the acquisition of Ferranti, says Padovani. The original Ferranti 3.5-μm linear bipolar process with toggle frequencies of 3 GHz was replaced by a more advanced 3-μm junction-isolated, ion-implanted, double-metal process featuring 15-V collector-emitter breakdown ratings and npn toggle frequencies up to 4.5 GHz. Excellent low-current properties make the process ideally suited for battery-operated or low-power designs.

The Ferranti-developed repeated-cell, or tile, architecture, permits 180° rotation of the metal interconnect pattern of a given macrocell, offering an alternate input/output position for a macrocell subcircuit. This scheme greatly facilitates cell placement and routing, Padovani says. Implementation of customer circuits is supported on industry-standard work stations with device models, symbols, and macro libraries, which include very fast comparators, video amplifiers, and low-noise op amps as well as general-purpose linear and digital cells.

As a modified npn, the monistor is actually a dual common-collector npn transistor with an additional p-type base region placed between the two npn bases. That setup allows the additional p-type base region to act as an emitter for lateral pnp transistor action, with the base number of standard-cell vendors, including Exar, LSI Logic, National, Sierra, TI, and VTC, are counting on various biCMOS semicustom strategies. "What biCMOS does for you on the performance side is to achieve the toggle frequencies associated with bipolar without sacrificing the density and power savings of CMOS," says National's Miller. "On the linear side, a bipolar transistor, even when scaled, offers much better analog performance than a comparably scaled CMOS device."

A major problem facing vendors of analog and mixed-mode semicustom methodologies is simulation, says Peter Hillen, director of strategic marketing at International Microelectronic Products. Where digital simulators need only describe the occurrence of a logic high or low at the output of a device, analog simulators must calculate the voltages, currents, and temperatures associated with these states, as well as the spectrum of voltages and currents developed by the device in the transition from one state to the other. And mixed-mode simulation, in which a circuit must be partitioned between digital and analog simulators, takes even more computer time.

On the analog side, most simulators use variations of Spice, an analog tool developed in the early 1970s at the University of California at Berkeley. "But Spice is slow and in some cases may not even produce a useful simulation," says Hillen. "One block to developing new simulators that are faster, more flexible, and easier to use is better device-level models." In particular, as transistors are scaled down in size and voltages reduced, new device models are needed to describe operation in regions of modest and weak inversion.

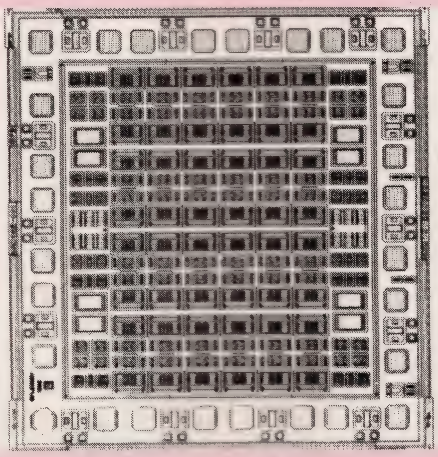
In mixed-mode simulation, there is a mismatch between the simulation time and acccuracy of the models. This forces the simulations to be done separately, with the output of one fed into the input of the other, and vice versa. "What is needed is an integrated simulation environment," says Hillen. Although some integrated simulators are starting to appear, he says, their performance is still less than ideal. "Until a satisfactory solution is forthcoming, simulation will be the bottleneck in most designs, and the source of considerable frustration."

Until a solution is found, 'simulation will be the bottleneck in most designs'

Until the simulation problem is solved, says MicroLinear's Gopin, perhaps the best idea is not to let systems designers get directly involved in the process at all. "The process of analog design, let alone simulation, is iffy and error-prone enough when trained engineers and analog designers are doing the work, with or without CAD tools," he says. "And the sources of error increase exponentially as you allow the outside system designer, unfamiliar with the intricacies of analog and mixed-mode design, into the loop." For this reason, he says, after about two years in the marketplace with a standard-cell mixed-mode CMOS library, MicroLinear has withdrawn from the market until better tools are ready.

The company is not abandoning standard-cell methodology, however. Instead, MicroLinear is using it internally as a tool with which its IC designers are developing custom circuits quickly. The approach is a vital element in a still-evolving semistandard product strategy, in which technologies from the company's semicustom and standard parts are woven together. "In the hands of an experienced IC designer, a standard-cell approach allows the development of a custom design in the turnaround time that approaches that of an array, but with the silicon efficiency of a full-custom design," Gopin says.

The semistandard strategy has been so successful in the standard-cell area that the company is extending the concept to its linear and mixed-mode arrays. In de-



Up to 2,000 devices fit on chips that team Plessey's "monistor" structure with a Ferranti architecture.

contacted at either of two locations. Alternatively, the monistor can operate as a standard twin-collector lateral pnp transistor on which the collectors have been enlarged to accommodate additional n+ regions.

Those regions serve as emitters for a vertical npn transistor. "Either way you look at it," says Padovani, "the result is the same: a compact merged transistor optimized for excellent operation as either a vertical npn or a lateral pnp transistor."

The array architecture is based on a minimal linear cell structure, which is repeated through the core of the array. The minimal cell structure is symmetrical about the x and y axes, thereby allowing the rotation of macrocell metal interconnect patterns. This symmetry provides a high degree of flexibility for circuit place and route.

IN THE CELL. The minimal cell includes four npn transistors, two universal monistors, and two resistor sections, each having one 8-kΩ, eight 2-kΩ, and four 500-Ω resistors. A peripheral cell structure that borders the core includes specialized component cells such as medium and large npn transistors, additional monistors, and capacitors.

The medium and large npn transistors are scaled at factors of about 6 and 12, respectively, with reference to the small npn of the core cell. These scaled devices are useful for bandgap references, low noise inputs, and high-current drivers. The capacitors can be metalized to obtain up to 7.5 pF of capacitance and are used primarily for circuit compensation.

The larger arrays will include digital cells to implement ECL or TTL logic and I/O buffers for control interface and to support analog/digital converter design.

Macrocells are facilitated by the symmetrical cell design and double-layer metal interconnects. These "metal macros" can be directly modified to customer applications and implemented immediately via a single metal mask, an advantage not possible with standard-cell design methodology, the company says. Work station support includes Analog Design Tools, PC Workbench, and Analog Workbench for Sun and Mentor Graphics. Support for Daisy work stations is planned in 1989. OrCad support is also planned for schematic capture on a PC. Full Spice models are available for virtually all versions. Automatic place and route is also being developed. Included in the cell library, which will be made available with the arrays, is a bandgap reference with an accuracy of 3% to 4% untrimmed and 1% trimmed; amplifiers with bandwidths of up to 500 MHz, 70 to 80 dB of gain, and 2 dB of noise; comparators with 5-ns delays; 100-MHz voltage-controlled oscillators; and phase comparators and drivers up to 100 mA and with slew rates to 200 V/μs.

The series includes the MFA with 12 analog cells and 109 transistors, the MFB with 24 cells and 200 transistors, the MFC with 36 cells and 302 transistors, and the MFD with 48 cells and 402 transistors. Also coming is the MFE with 36 analog and 10 ECL digital cells and 696 transistors. *–B. C. C.*

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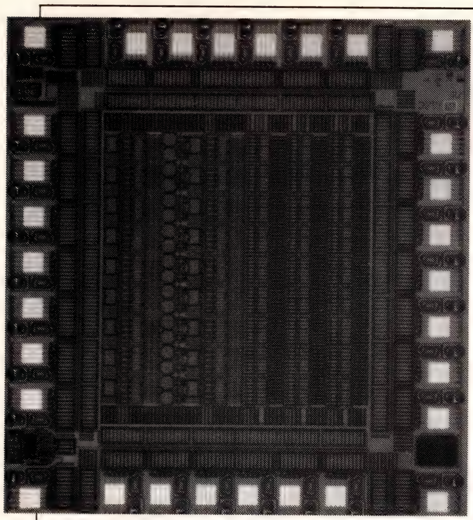


Maverick Plessey offers 18-V CMOS analog/digital arrays; most arrays are bipolar.

velopment is the first in a family of semistandard linear core-based products. Built with the same 40-V process used in the 3600 series of arrays, each semistandard part is built around a core cell incorporating an industry- or market-specific analog function. The core is surrounded with a variety of hard-wired macrofunctions with a variety of peripheral functions that the system designer can add or subtract by filling out a simple form attached to the specification sheet for the part. After that, says Gopin, the company will turn around a completed design within a few weeks.

Advanced Linear Devices Inc. of Sunnyvale, Calif., has also developed a semistandard approach. Its methodology retains the advantages of the semicustom standard-cell approach; however, it eliminates the need to put sophisticated CAD layout and simulation tools into the hands of the system designer. The company has developed what it calls a function-specific 3-μm, 12-V analog CMOS standard-cell family; all of the cells in its library are also available as standard parts from the company. In addition, there are 86 analog and digital functions available as standard parts with guaranteed specifications in a kit that also includes data sheets and a design manual, says Michael O'Neal, vice president of marketing.

BREADBOARD. Once the system designer has completed a breadboard specific to his requirements and determined a pinout and a package type, the package is handed over to the company's circuit designers, who use handcrafted standard-cell equivalents to build a custom circuit. This approach, says O'Neal, virtually guarantees first-time success of a custom chip, while allowing for circuit refinement by using the initial breadboard in the system, prior to committing to the finalized cell-based design. Further, since there is no hardware or software to buy or learn to use, and the user does not get involved in IC design or layout, considerable customer engineering time and cost savings are realized.

One company with a semistandard strategy wants to do it all, and that's Exar. It is using both its N2000 standard-cell CMOS family and its linear bipolar Flexar Delta series of arrays for internal development of standard and custom products as well as offering it to customers, says Exar's Ihan Refioglu, vice president of marketing. What this will give Exar is flexibility, he says. "If one approach does not fit the cost and turnaround [needs] and expertise level of the potential user, maybe another will," he says. "The more options you can offer, the more likely you are to make a sale." ☐

IMP MAKES A BOLD MOVE WITH CMOS PROCESS

As its competitors dip cautiously into the marketplace with mixed analog/digital standard-cell offerings, International Microelectronic Products Inc. is jumping in with both feet.

The definition of caution in the market for analog/digital application-specific integrated circuits is the decision to add increments of analog capability to a standard digital CMOS process. The San Jose, Calif.-based custom/semicustom IC house has done just the opposite, developing a CMOS process that yields analog performance as good as that yielded by some bipolar approaches, and using it to build digital circuitry in addition to analog circuitry.

IMP has also been bold in terms of device feature sizes, in the push for high density. The safer approach of some analog ASIC houses has them using conservative 2- or 3-μm design rules. IMP has leapfrogged not only over them, but also over the 1.5-μm digital standard-cell offerings, bringing to market an aggressive 1.2-μm library of analog and digital cells and macrocells.

An aggressive 1.2-micron library of analog and digital cells is on the way

Another advantage IMP offers is an optional process module that adds biCMOS to the mix without the many costly masks that conventional biCMOS designs require. Another process module is in development that will add 10-V capability, which will come in handy for the company's planned electrically erasable programmable read-only memory cells, as well as for other applications.

Compared to many competitive mixed-mode, standard-cell offerings, IMP's new libraries offer twice the system speed (a 40-MHz digital clock versus 20 MHz for 2-μm CMOS) and as much as twice the density, says Peter Hillen, director of strategic marketing. Traditional CMOS applications that will benefit from the new capability include modems, transceivers, and multiplexers for telecommunications, says Hillen. "Also, because of their higher digital speed and analog throughput, applications traditionally dominated by bipolar arrays—such as video [digital-to-analog converters], disk-drive electronics, and consumer video and radio—are also opened up," he says.

IMP's process has allowed the design of a variety of high-performance analog cells not previously possible in CMOS, claims Thomas Flageollet, product marketing manager. These include operational amplifiers with gain-bandwidth products as high as 300 MHz, latch comparators as fast as 6 ns, DACs with 100-MHz conversion rates, and switched-capacitor filters capable of operating at the frequencies used by consumer radio and television equipment.

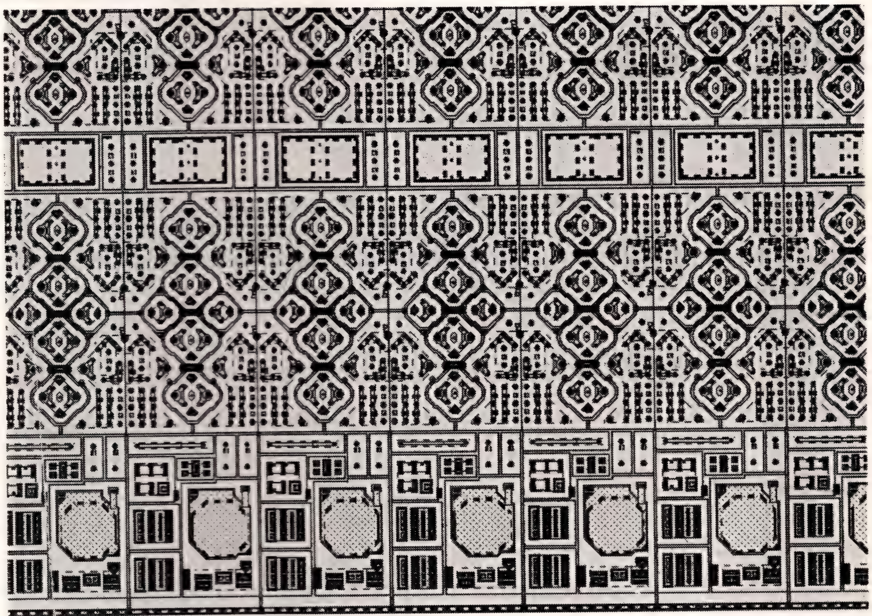
Key to this high performance level, says Hillen, was a shift from the p-well CMOS process, common to many mixed-mode designs, to an n-well process. This has three benefits: lower noise, higher performance, and compatibility with current EEPROM memory technology.

The use of an n-well CMOS process was also important to achieving the speeds usually associated with bipolar linear processes, because it allowed the company's designers to implement biCMOS chips without any additional fabrication steps or costs. IMP has managed this miracle by taking advantage of the parasitic bipolar npn transistors that occur as a byproduct of conventional CMOS processes.

Such parasitic structures have limited usage, especially in p-well-based processes, because they are common-substrate devices with only two terminals. To get fully functioning three-terminal devices, in most implementations it is necessary to add a number of processing steps. But by shifting to an n-well process, says Hillen, it is possible to build fully isolated vertical npn transistors which use the well as the collector and a separate diffused layer for the base.

About 50 cells in the more easily characterized digital-cell library are currently available to outside customers. Cells in the analog library are now being characterized and used internally. Among them are five op amps, three comparators, voltage and current references, and more complex macrocells, such as data converters. The analog cells will be available by December. *–B.C.C.*

EXAR DRIVES DOWN THE COST OF ARRAYS



The Flexar Delta analog/digital bipolar arrays allow the user to select the length of the chip in one-cell-width increments, so wasted silicon can be kept to an absolute minimum.

Exar Corp.'s second-generation version of its Flexar analog/digital bipolar array could fundamentally change the economic equation between full custom and semicustom. The Delta-series arrays feature selectable die size and multifunction components that can be used for analog, digital, or mixed-mode designs. The basic approach is so flexible and silicon-efficient that it could make bipolar semicustom arrays competitive for the first time with full-custom chip designs when production requirements hit high volumes—up to 1 million units—the company says.

"When we introduced the original Beta-series Flexar arrays in 1986 we changed the [economic] crossover point between semicustom and custom to 250,000 units from 50,000," says Ilhan Refioglu, vice president of marketing. "This has been increased fourfold with the Delta series through a reduction in die size of about two-thirds, increased component flexibility and functionality, and mixed analog/digital capability."

To obtain these advances, the San Jose, Calif., company uses a symmetrical cell structure that incorporates multifunctional transistor elements that can be programmed to fit user requirements. What's more, because the basic cell is symmetrical, the array can be interconnected much more efficiently and can be stacked in single-cell increments. That makes it possible for a designer to specify the die size exactly at the final mask step so that the circuit will include only the components required by a given application.

Initial members in the new family include the Delta 2000, with up to 440 transistors and a total of 1,310 passive and active components, and the Delta 4000, with 760 transistors and 4,900 components. Both are fabricated using a new 3-μm bipolar process compatible with both standard and differential current-mode and emitter-coupled logic and are capable of 1-GHz toggle rates.

Typical nonrecurring engineering costs for a Delta series design will range from $20,000 to $50,000, with a turnaround time of three to eight weeks. High-volume per-unit costs for smaller arrays are estimated by Exar at about $1, a savings of 25% to 30% over previous semicustom arrays. Per-unit costs are also only about 10% more than a comparable circuit implemented using a full-custom methodology, and the new Delta-series arrays require no more than 10% to 35% additional die area than a full-custom solution.

In the Delta-series arrays, there is little loss in silicon efficiency no matter whether the design is full analog, digital, or mixes the two, says Refioglu. In the 4000, for example, the designer has the choice of integrating 16 operational amplifiers of the 741 type, or 33 D-type flip-flops, in a single chip. The designer can use either fast nonsaturated CML or ECL, as well as four to eight times the amount of circuitry that can be fit on other analog bipolar arrays, Refioglu says.

Flexar arrays compete with full-custom chips in volumes as high as a million units

The Delta series resolves a number of major problems facing previous bipolar tile-based semicustom alternatives. These approaches resulted in much larger die sizes, and thus higher costs in volume productions, than full-custom designs. In previous tile-based approaches, the die contains a fixed set of components. As a result, if the fixed mix of npn and pnp transistors and other components does not fit a particular design's requirements, many components—and square mils of silicon area—go to waste.

And in the tile-based approach, if a design requires more circuitry than is provided on the chip, silicon area must be added or external components used. And because the functions are fixed, routing the interconnect is inefficient, requiring die sizes that are often two to three times larger than the same function would need in a full-custom design.

Introduced in 1986, the original Flexar Beta series only partially addressed these problems, Refioglu says. The Beta series used a proprietary multifunction transistor structure, the Twinstor, which featured programmable npn and pnp transistors and bonding pads and no fixed-location passive components. This multifunction transistor solved the problem of inefficient usage of the tiles by allowing structures to be modified to fit the users' requirements.

But the original Twinstor element was basically a nonsymmetric rectangular structure, making for inefficient routing of interconnect lines, says Giovanni Giannella, group manager of engineering operations and inventor of the Flexar linear-array concept. In addition, the number of basic transistors remained the same, no matter whether the designer needed them all or not, Giannella says.

SYMMETRICAL MACROCELL. In the Delta series of arrays, the basic building block is a symmetric hexagonal macrocell with two equally populated subcells (see drawing, p. 84). Each subcell contains two structures called Twinstors (T_1 and T_2), each of which can be programmed four ways: as two npn transistors with a common collector, one pnp transistor with a dual collector, two matched resistors, or a crossover resistor. With a breakdown voltage of 20 V, says Giannella, the Twinstor can be used for the majority of linear applications. Each Twinstor is a merged structure in which the bases of two vertical npn transistors are fabricated on the same island so that they can be used as collectors of a lateral pnp transistor.

An additional p-type area is diffused in the center, between the two npn bases, to act as the emitter of the lateral pnp device. One advantage of this structure, says Giannella, is that the base regions can be used as two matched low-value resistors, about 200 Ω each, increasing the cell's functionality and flexibility. Located between the two Twinstor subcells are two spare npn transistors (T_3 and T_4 in the drawing) that can be used when only one or two additional transistors are required to complete a function, eliminating the need to use an additional cell. Each subcell also has two transistors (T_5 and T_6) specifically for use as emitter-followers, which eliminates the need to use much bigger and isolated transistors.

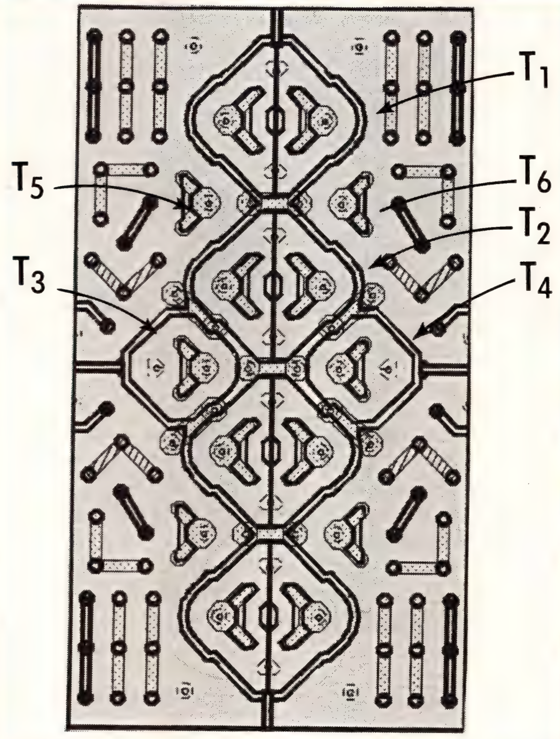
Compared with conventional tile arrays, the cells in the Delta series are extremely flexible and silicon-efficient. For example, when used as an analog element, one cell can implement a simple op amp, and two cells can be used to build a more complex 741-style op amp, says Giannella. In addition, the basic cell can be broken up into subcells, each one forming the building block of any analog design, a differential pair with its own current source. As a digital element, a single cell can be configured as four gates with dual inputs and an emitter follower, or using cascoded ECL, as a D-type flip-flop.

Because digital applications require much higher routing capability than linear applications, routing channels for power-supply and signal lines are placed between rows of cells. To avoid wasting this significant silicon area in analog applications, the routing channels are also used for building customized oxide-dielectric capacitors where the value of the capacitor is a function of the channel's length and width.

RESISTORS AND ZENERS. In applications such as analog-to-digital and digital-to-analog converters, as well as precision references and similar circuits, where high-precision ratios and low temperature coefficients are required, thin-film resistors can be deposited in the same areas. The resistors can be trimmed using zener diodes that are available in special peripheral devices located around the edges of the array—structures called Padstors. Each Padstor can be configured as a standard bonding pad; a medium-current npn or pnp transistor; a capacitor; or as a zener network, as well as a bonding pad with 2,000 V of electrostatic-discharge protection.

In each Padstor, the npn transistor can be configured as either of two types of capacitor. The first type is an oxide capacitor formed by the common method, with one plate consisting of the aluminum metalization and the second a diffused area. The second is a junction capacitor formed by diffusing a p+ area under the bonding pad, automatically creating a capacitor within the n-type epitaxial layer. By connecting the top plate of the oxide capacitor to the epilayer where the p diffusion is located, the two capacitors can be used in parallel.

A FLEXIBLE BUILDING BLOCK



The Twinstor structures (T_1 and T_2) in each half of a macrocell can be used as a pair of npn transistors or a single lateral pnp transistor.

Taking advantage of the dual symmetry of the basic cell, Exar designers have configured the Delta 2000 and 4000 to allow the designer to customize the die in a single metal-layer mask step. This is done by repeating a basic row of a predetermined width (two cells wide for the 2000 and four cells for the 4000), continuously along the wafer, with no interruption and no scribe line. The width of the array is fixed, with predetermined locations for Padstors, bonding pads, and scribe lines along the horizontal axis. But along the vertical axis, the Padstors are placed only when the array's length, and thus the overall die area, have been determined for a given design.

Using no more process steps than a single metal mask, says Giannella, the user can select the length of a Delta 2000 design to vary its size over a wide range. The transistor count can be selected from 22 to 418, and die size from a minimum of 25 by 61 mils to a maximum of 179 by 61 mils. In the Delta 4000, the number of transistors varies from 76 to 1,292 and die size from 102 by 34 to 102 by 306 mils. The number of rows is variable from 3 to 21 in the 2000 and from 6 to 36 in the 4000.

This approach allows the customer a nearly continuous choice of array sizes, where the difference in component count between successive increments in die size is usually no more than 10%, says Refioglu. In conventional tile arrays with fixed die geometries, the size difference between two successive members of an array family can be as much as 50%.

Based on the company's 10 years of experience and more than 1,000 full-custom designs, Refioglu feels confident that the new generation of Flexar arrays addresses about 90% of the applications that are targeted for full-custom implementations. But there is considerable room for growth in several directions, as the market expands and new applications demand it, he says.

For example, wider arrays with up to eight cells per row and 800 transistors are under development, says Refioglu. Also being considered are arrays that are programmable in both width as well as length. A natural migration path from this would be to higher frequency, such as to 3.5 GHz. "I feel we are at the edge of the wave [of market demand in analog semicustom arrays] and I want application customers to push me in the right directions rather than for me to dictate the market requirements," Refioglu says.

But after moving to higher frequencies in the 2.5-to-3-GHz range and toward higher densities in bipolar technology, the next step would be a biCMOS array, he says. The plan would be to use mixed bipolar and CMOS elements in the array for high-precision linear functions and CMOS for the digital functions. That kind of product could be ready as early as late next year, but Exar is still waiting to see what potential market demand will be before committing to dates, Refioglu says. "This is strictly a business decision. Technology-wise we are there," he adds, with a 2-μm, 11- to 18-mask, double-metal, double-polysilicon, n-well biCMOS process used in its N2000 standard-cell family and for some standard products. *–Bernard C. Cole*

EXAR'S CHIP STRATEGY TAKES WIDE AIM

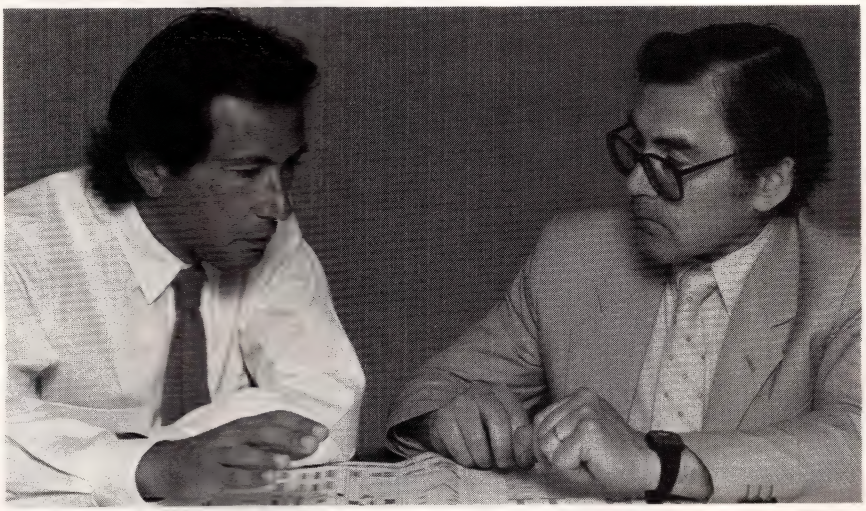
Analog semicustom technology has come of age, says Ilhan Refioglu, vice president of sales and marketing at Exar Corp. And what's in demand are integrated-circuit fabrication methodologies that combine analog and digital circuitry on the same chip. So Exar is putting the finishing touches on a multipronged strategy designed to take advantage of that.

The San Jose, Calif., firm is going after both the bipolar, high-performance part of the business and the high-density CMOS segment. Its strategy is different from many competitors in analog and digital application-specific ICs—most are focusing on either segment, but not both. At the same time, Exar wants to play both sides of the chip-market fence, offering both semicustom products and standard parts.

Exar is depending on two new semicustom families to achieve its ambitious goals. The families are the result of 8 to 10 man-years of development effort and a heavy investment in research and development, Refioglu says. The total spent to date on developing the Flexar Delta bipolar analog/digital array series and the N2000 biCMOS standard-cell line has been about $1.5 million, split equally between the two over the past two years, says company president Nobuo Hatta.

The Flexar Delta arrays are very important to the company, says Hatta, establishing its leadership in the bipolar linear-array market and gaining Exar entry to the $900 million custom linear market with a cost-effective alternative. But for the long-term viability and growth of the company, it became clear several years ago that the even larger market for analog/digital CMOS products was just as important, says Hatta. The success of the two semicustom product lines, bipolar and CMOS, will account for much of the growth of the company, he believes.

If all goes well, Hatta thinks Exar will grow at least 20% to 25% per year through the mid 1990s. "In particular, we expect the dual capabilities to open up new opportunities in the higher-volume consumer and automotive markets," both for semicustom sales and for proprietary standard products built with the same tools. He also expects a significant increase in sales in Japan and Europe.



Exar's head of marketing, Ilhan Refioglu (left), and Giovanni Giannella, inventor of the Flexar linear array concept, expect new markets to open up to the company's technology.

BIPOLAR AND BICMOS. The Flexar Delta bipolar arrays target the high end of the market, where the basic requirement is to integrate high-performance analog functions on the same chip with a small amount of digital circuitry. At the lower-performance end of the business, where there's a need to integrate almost as much digital as analog circuitry, the company has developed the biCMOS N2000 family.

Key to the company's success in biCMOS, says Hatta, is its analog expertise. Instead of developing a 5-V process compatible with digital CMOS, Exar chose to build around its traditional strengths with a 2-μm, 20-V modular biCMOS process and a library of standard cells.

The N2000 biCMOS family contains 20 electrically erasable programmable read-only memory cells, in addition to incorporating a cell library of more than 30 analog cells and 100 digital cells. "We expect this unique combination will open up new market areas in the automotive, industrial, and medical arenas," Refioglu says.

It's competing in bipolar and biCMOS semicustom arrays, as well as standard parts

He adds that having the EEPROM cells also gives the family an extra dimension of design flexibility, because the ability to modify designs through reprogrammability can yield the cost advantages of more generalized semicustom solutions.

The latest Exar development, however, is the Delta bipolar series, which features on-chip programmable multifunction components for analog, mixed-mode, or digital circuitry. It can also be customized by the user to achieve the most cost-effective die size possible.

This high degree of programmability means that a bipolar array buyer, who might once have found a full-custom solution more cost-effective at a production volume between 50,000 and 100,000 units, gets a savings with the semicustom chip at up to a million units, Refioglu says.

Although the main focus of the Delta and N2000 families is in the semicustom arena, Exar also plans to take advantage of their capabilities in its application-specific standard-product line. Employing a semistandard strategy, Refioglu expects to use both families to accelerate and reduce the company's time to market in such key areas as telecommunications, data communications, and microprocessor peripherals.

"In the past, the synergism between our custom/semicustom and standard-product efforts was a one-way street, with many of the standard products or subsets thereof becoming elements in our cell library," says Giovanni Giannella, group manager of engineering operations. "With the improved speed and density of both the bipolar arrays and the biCMOS standard cells, we expect to take advantage of these capabilities to get [standard parts] to the market one step ahead of the competition."

As the two new families go into wider use, both within and outside the company, Refioglu expects semicustom and standard-part sales to grow in excess of historical rates. In fact, he says, it is already happening. An increase in sales of almost 20% is expected in 1989, to $50 million, from $42 million in 1988. The company is projecting a 15% hike in 1988 over the previous year. And where 60% of the company's business is currently focused in such areas as microprocessor peripherals, data communications, and telecommunications, Refioglu expects to see increased penetration of applications that have been predominantly custom-oriented—automotive, consumer, industrial, and medical. *–B.C.C.*

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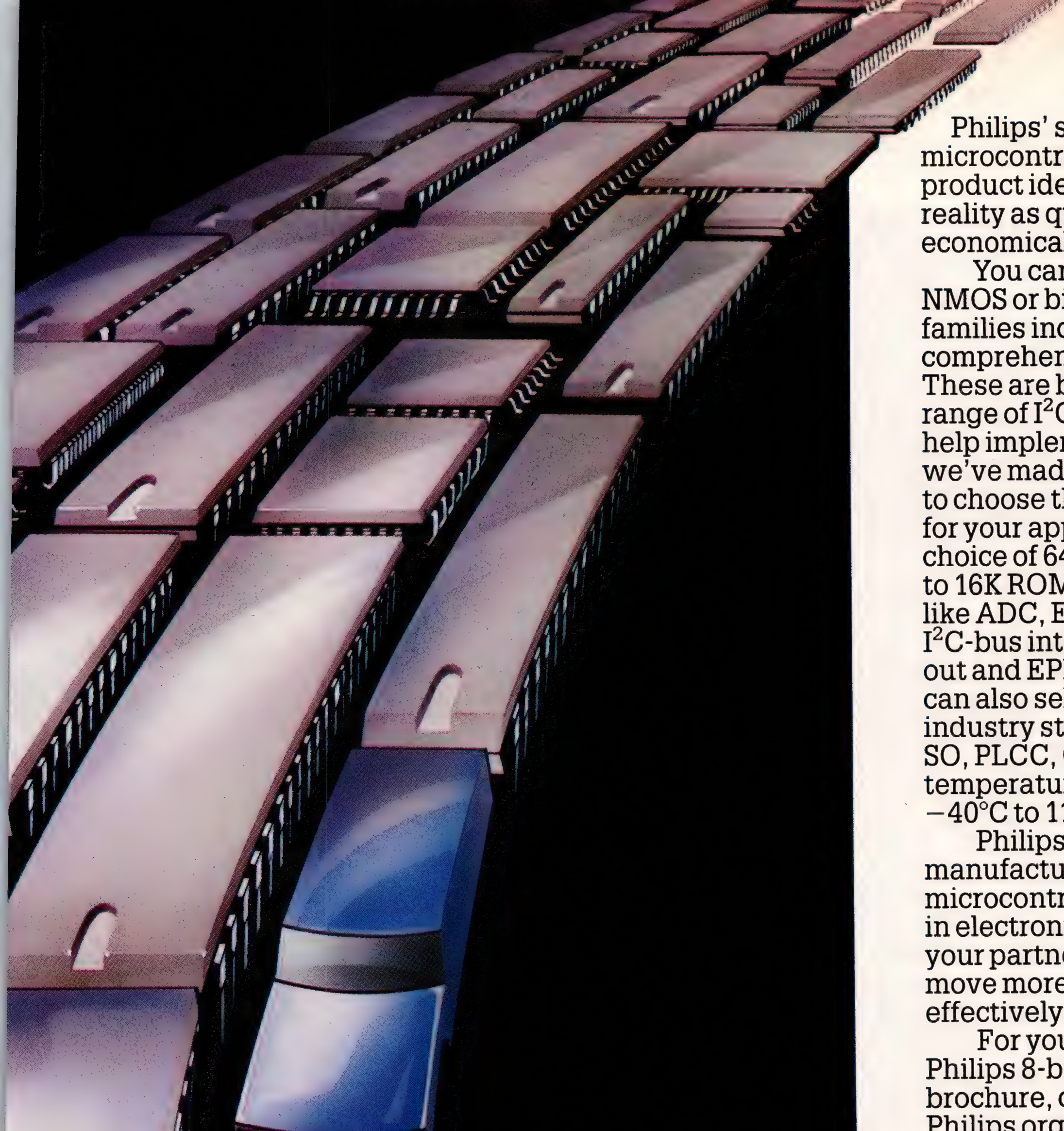

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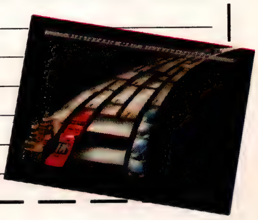

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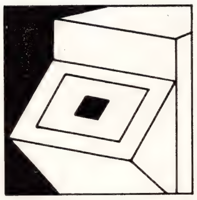
GROWTH SPURT OPENS THE DOOR FOR U. S. VLSI TEST SYSTEM MAKERS

As the high yen holds back the Japanese, innovative U. S. vendors try to regain market share



U.S. makers of VLSI test systems are moving to get back market share lost to Japanese companies. The time is ripe, U. S. manufacturers believe, because most of the markets they compete in are surging in growth, although the pace will probably slack off by 1990, analysts say. While the market is perking nicely in response to hot semiconductor markets, the high value of the yen is at the same time making it harder for Japanese vendors to compete. So U. S. companies are playing their best hands, trying to seize the initiative.

Advantest Corp. of Tokyo, formerly called Takeda Riken, is the Japanese company that has cut most heavily into market share held by U. S. test-system makers the last five years. "It's the company to beat," says G. Dan Hutcheson, president of VLSI Research Inc., San Jose, Calif., a market-research concern that follows the automatic-test-equipment business. He says that in a market driven by technology, Advantest—which has a U. S. subsidiary, Advantest America Inc., in Lincolnshire, Ill.—has kept up a fast introduction pace for new leading-edge products.

BIGGEST MARKET. But U. S. manufacturers are not standing still either. Important innovations developed by U. S. companies, such as tester-per-pin architectures and close links with computer-aided-engineering tools, are becoming important factors as those vendors attempt to turn around the market-share battle.

The most hotly contended segment—also the largest and fastest-growing segment—is logic test systems, where Teradyne and LTX are scrapping it out with Advantest and Ando. The U. S. and Japan each dominate one of the two biggest remaining segments. The market for linear test systems, and mixed analog/digital, is still neatly in the pocket of U. S. manufacturers. Japan, which makes most of the world's memory chips, holds sway in the market for memory test systems, however. Both those segments are also growing well and will continue to do so through 1990, if industry projections run true.

It's a welcome change. The ATE business looked like it was going down the drain during 1985 and 1986, after a high-water mark in 1984. The 1984 worldwide market for semiconductor test systems was worth $995 million, but fell to $989 million in 1985 and then plummeted to $837 million in 1986, according to figures from Mabon, Nugent & Co., a New York investment firm. In 1987, the market finally turned around, seeing 7% growth over 1986 figures.

VLSI Research is now bullish on the overall component test business. The market-research firm sees the semiconductor tester market climbing back to $944.8 million in 1987 (see chart, p. 90). Of the five major segments—logic, memory, linear, discrete, and burn-in systems—logic testers represent the lion's share, nearly half the dollar volume of component test systems shipped. Linear testers constitute just over 20% of the sales volume while memory testers come in third with just over 17% of the total revenue.

Logic, linear, and memory test systems will all grow rapidly in 1988: 54%, 39%, and 38%, respectively, VLSI Research predicts. It then sees growth tapering off to more normal rates in 1990—16%, 22%, and 19% for the logic, linear, and memory segments. It attributes the current surge in growth to two factors. One is that chip makers who had deferred capital-equipment expenditures during the chip downturn came back into the market this year. Growing demand for the latest generation of VLSI devices is the other factor spurring demand, says Hutcheson.

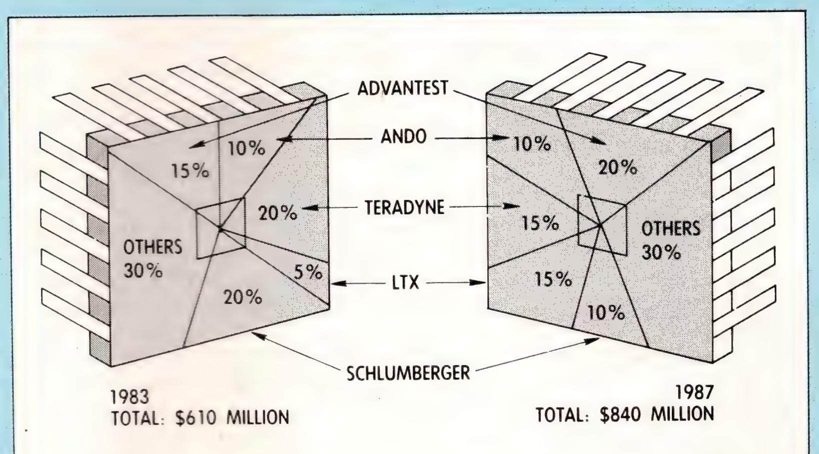
Sales for VLSI test systems has built-in inertia for the next year or so, thanks to the semiconductor's industry pell-mell race to develop devices with higher integration levels. The installed base of test systems will become obsolete as more complex chips are developed, says Frederick Wolf, an analyst with Mabon Nugent.

The market for high-end VLSI testers will grow as much as two times faster than the semiconductor industry over the next few years, he says. So even if there is a recession in the semiconductor business, VLSI chips already developed will sustain demand for test systems they ramp up into volume production.

The biggest, fastest-growing market segment—logic testers for LSI, VLSI, and application-specific ICs—is where Advantest has been making its biggest mark. Both Advantest and Ando are now well entrenched in the U. S. part of the market. "Advantest has over 50 systems at AT&T and IBM and 30 systems at Digital Equipment Corp.," says Raj Rajaratnam, an analyst with Needham & Company, Inc. in New York City.

Ando Corp., Tokyo, is not doing as well as Advantest, says Hutcheson of VLSI Research. "Ando was doing well but the company got too high up on the technology curve and the cost of its systems started to rise," he says. "Then when the yen

HOW JAPAN'S VLSI TEST MARKET SHARE GREW



SOURCE: VLSI RESEARCH INC.

went up, its cost were out of line with what customers wanted to pay."

Advantest, on the other hand, was better positioned when the yen went up because the company had begun manufacturing testers in the U. S. It was the first Japanese semiconductor test equipment maker to do so.

But U. S. companies are now in a position to compete strongly with both Japanese firms, thanks to their technical innovation and the higher value of the yen. The Trillium subsidiary of LTX Corp., a San Francisco-based specialist in VLSI logic testers, is one the brightest U. S. stars. "Trillium pioneered the software interface between the tester and the CAD work station," Hutcheson says. And Megatest Inc., San Jose, Calif., though still small, gets big credit for innovation. "Megatest developed the tester-per-pin architecture," says Hutcheson. "Every test company today recognizes the architecture as the next major step for ATE." And he credits Teradyne Inc. of Boston with pioneering equipment for microprocessor testing.

LEADERSHIP. This technical prowess has not gone unnoticed among ATE customers. In a survey of ATE customers VLSI Research carried out, it asked respondents to rank ATE companies in terms of technical leadership. LTX/Trillium came in first, Teradyne second, Megatest third, Micro Component Technology Inc. of St. Paul, Minn., and Advantest tied for fourth, and Schlumberger/ATE, San Jose, Calif., was fifth. In terms of product performance, those surveyed ranked Advantest and Teradyne together, tied for the top spot. LTX/Trillium came in second and Hewlett-Packard third.

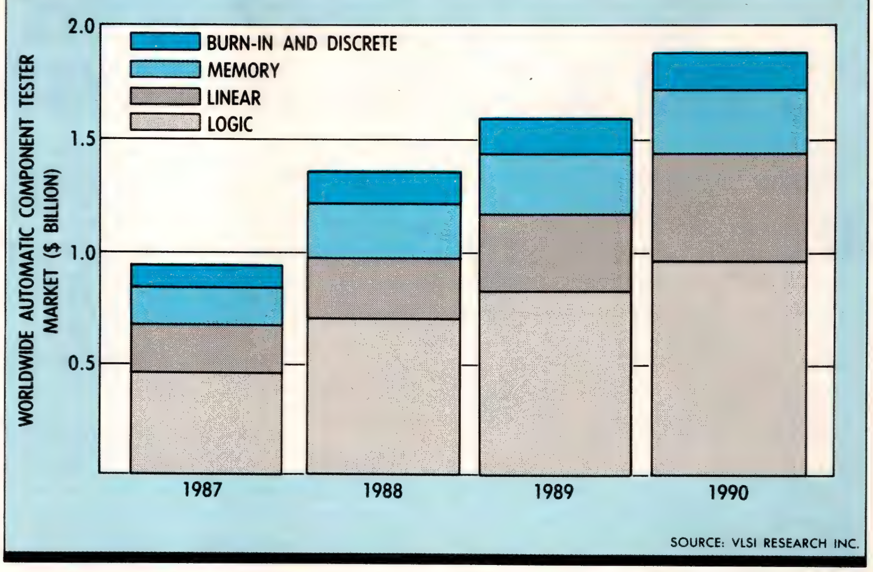
ATE users have spoken with their orders, too. Intel and National Semiconductor have chosen Trillium to test their 32-bit microprocessors, Rajaratnam says. "We estimate Teradyne has sold six J953 systems, a couple to Advanced Micro Devices, one to ITT, and others to MIPS Computer, Delco, and Chrysler," he adds.

Motorola Inc. is also looking for a new system for testing microprocessors and digital-signal-processing chips because GenRad, which had the Motorola account, withdrew from the component test business. Teradyne and Trillium are duking it out for the Motorola business, says Wolf.

Trillium recently won a similar competition with Teradyne to get the Intel business. That was bad news for Teradyne, because the semiconductor giant represents 30% of Teradyne's business, Rajaratnam estimates. On the other hand, Delco, which was another GenRad account, went with Teradyne.

Logic testers are the biggest sellers now, but mixed-signal testers may soon start growing faster. By 1991, mixed-signal devices will represent just over 40% of all VLSI ASIC devices produced, predicts Michael Kondrat, marketing manager at the semiconductor test system division of Tektronix Inc. in Beaverton, Ore.

GROWTH WILL TAPER OFF IN 1989



SOURCE: VLSI RESEARCH INC.

The two companies now dominating the segment that includes both mixed-signal and linear-only testers, says Wolf of Mabon Nugent, are: LTX with 45% and Teradyne with 30% of the dollar volume shipped. Curiously, although a significant portion of linear ICs are made in the Japan, no Japanese ATE company has challenged the U. S. dominance.

LTX and Teradyne are butting heads over the lead position. "Teradyne has attacked LTX's leadership position in this market segment with their A500 mixed-signal tester and have about a dozen orders from companies such as AT&T, Siemens, Texas Instruments, Analog Devices, among others," says Rajaratnam [*Electronics*, Jan. 22, 1987, p. 55].

Logic test systems, the most hotly contested area, is also the fastest-growing

The price tag of the A500, $1.5 million, is steep; to better satisfy customers who did not need all the A500's capability, Teradyne recently rolled out the A510, which sells for $1 million. To attack LTX's position in the linear-only test market, Teradyne also introduced a linear tester with no mixed-signal capability, the A520.

"The LTX response to the A500 is the SynchroMaster, a 50-MHz system offering between 64- and 256-pin test capability. It combines the architecture of their linear tester and the Trillium machine—their VLSI test system," Rajaratnam says. "LTX has a couple of orders, one from Northern Telecom, but won't start shipping the machine until October 1988."

Just as higher-technology mixed-signal chips are driving the linear segment of the tester market, next-generation dynamic and static random-access memories are driving the demand for memory testers. With the surge in production of 1-Mbit DRAMs and 256-Kbit SRAMs and the pending production of 4-Mbit DRAMs and 1-Mbit SRAMs, chip makers are hungry for next-generation memory testers. And the action is in Japan.

Ando will experience a growth rate of 60% in the Japanese markets this year, a large share of which is spurred by sales of memory testers, says James Mulady, manager of sales and marketing at Ando's Sunnyvale, Calif., subsidiary. "We have gone through the generation of 10- and 25-MHz memory testers, and we are now embarking on the 50-MHz generation," he explains. The demand for this class of tester is being driven by 1- and 4-Mbit DRAMs with access times under 70 ns and high-density SRAMs with access times of under 35 ns.

"In the memory tester market segment, Advantest is the market leader and Ando is in second place," says Mulady. The largest shareholder in Advantest is Fujitsu, and the largest shareholder in Ando is NEC. These shareholders dominate the board of directors but do not control the operation of the ATE companies. Nevertheless, Advantest has the memory test business at Fujitsu and Ando the memory test business at NEC.

Only one U. S. ATE company is making inroads at all into the Japanese market. Wolf says Teradyne's J937, introduced in 1986, is more advanced than Japanese offerings and was targeted to test 4- and 16-Mbit DRAMs. Thus far, he says, only two systems have been sold to Japan—one to Hitachi and the other to a company he could not name. *–Jonah McLeod*

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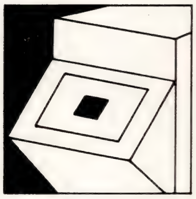
TEST-SYSTEM MAKERS RISE TO THE BIG-ASIC CHALLENGE

Test systems for ASICs are finding new ways to climb today's heights of complexity and speed

by Jonah McLeod



The automatic-test-equipment industry is working hard to accommodate the accelerating demands of a fast-growing segment of the component market: application-specific integrated circuits. System houses everywhere are turning to ASICs, and ATE vendors are responding with new strategies and technologies that target gate-array and standard-cell parts with ever-higher speeds, complexities, and pin counts. Many such developments in ASIC testing will be in evidence at the International Test Conference in Washington, D. C., to be held Sept. 12-14.

One approach now being touted for ASICs is level-sensitive scan design, which adds scan-path circuits to chips solely for test purposes. The scan-path strategy delivers a more complete test of a complex chip, and does it in less time. The general approach was developed more than a decade ago, but its use has been limited because of significant sacrifices in performance and chip real estate. But the magnitude of these sacrifices has been reduced. What's more, design tools are making test generation automatic for chips using scan methodology.

Vendors of test or verification systems for ASICs are also moving fast to optimize their systems for ICs with higher gate and pin counts. In looking to the future, they see a crucial need to be able to add pin-count capability—and the associated high-data-rate capability for test patterns—easily and at low cost. Modular test-system architectures are key to achieving this goal.

Increasing pin counts in ASICs are forcing another trend in test systems, the move to wafer probing. Chip packages with very high pin counts are more expensive than the chips themselves, so it makes good economic sense to test the chips on the wafer, and package only the functioning ones. New probes are making it possible to test the ac characteristics of chips before they are packaged.

SPEED TEST. Yet another group of test companies is working on the problems of testing very fast ASICs—gate arrays made with emitter-coupled logic and gallium arsenide. Photon Dynamics Inc., a startup in San Jose, Calif., has a new system based on laser technology that affords data rates, timing accuracy, and resolution ten times better than conventional ATE systems.

The bulk of the ATE world's attention, however, is focused on the high-complexity, high-pin-count end of the ASIC spectrum. In 1983, the largest ASICs built contained 9,000 gates and had 120 input/output pins. "Today our high-end ASICs contain 100,000 gates and need nearly 400 pins," says Jerry Rau, product manager LSI Logic Inc. in San Jose, Calif. "By 1990, the biggest devices will contain 200,000 gates and need over 500 pins. If such chips are to be tested efficiently, testability must be designed in."

Enter scan-path technology, which has seen limited use because of its associated drawbacks in chip area and design difficulty. Adding scan circuits to designs in the past has increased chip area by as much as 30% and slowed designs down significantly, adding several nanoseconds to gate delays.

But one newcomer to the ATE market, Gillytron Inc. of San Jose, Calif., along with its development partner, ASIC vendor Integrated CMOS Systems Inc. of Sunnyvale, Calif., is making these tradeoffs far more favorable. Gillytron's test system is relatively inexpensive—yet the system tests an IC just as thoroughly as its high-priced relatives (see p. 100).

The ScanMaster DV-8005 is a test system built specifically for testing ASICs with scan design built-in. The system can be configured with as many as 1,792 I/O pins, each with 1 Mbit of memory to handle the long scan patterns involved. In operation, the tester serially shifts in scan

HP's UPSCALE VERIFICATION SYSTEM PUTS AUTOCALIBRATION TO WORK

As the pin counts and clock speeds rise in the world of application-specific integrated circuits, makers of ASIC-verification systems are finding themselves hard-pressed to provide the combination of accuracy and high-data rate needed to debug these designs. Systems on the market now generally can only provide testing speeds of up to 100 MHz and timing accuracy of around ±500 ps. In some cases, system accuracy is only ±1,000 ps, barely sufficient to handle emitter-coupled-logic gate arrays operating at 100 MHz.

To address this problem, Hewlett-Packard Co. of Palo Alto, Calif., is launching a new verification system, the 82000 IC-evaluation system. Due for first shipments in the first quarter of 1989, it operates at 200-MHz data rates across all of its 384 test pins. In addition, the system affords a ±250-ps overall system accuracy, an accuracy that is maintained with automatic calibration capability. The system also boasts five different data formats that are usable at its full data rate; this makes it possible to test more kinds of ASICs.

Advanced wideband ECL driver/receiver electronics give the system its muscle

Advanced wideband ECL driver/receiver electronics are behind the system's high-data rate. This circuitry incorporates some of the high-speed pulse-generation capability built into other instruments from the company, such as its high-accuracy 1-GHz pulse generator. This high performance comes in a tester-per-pin architecture, a type of test-system design being used in many new-generation products because of the added efficiency it brings to the test process.

Some ASIC verifiers that are on the market can achieve high data rates, but only by employing multiplexing driver/receiver cards, a method HP has avoided in the 82000. In a 256-pin multiplexed tester, for example, a test system might be able to apply data to all 256 pins of a device at a data rate of 100 MHz. To run at 200 MHz, the outputs of pairs of driver/receiver cards are multiplexed together to double the tester's data rate. This is an inexpensive route to higher test speeds, but it cuts the pin-count capability in half.

data on selected I/O pins of the device to an internal scan ring, which sets internal nodes to a known configuration. The ring is a serial path that snakes its way through a selected number of flip-flops in the chip—or all of them—as determined by the designer. When the tester has set the internal nodes to the desired state, it then applies a stimulus to the chip's I/O pins. In addition to the response on the device's output lines, the response captured at nodes inside the chip can be checked by serially shifting data out the scan line.

Although a system like Gillytron's is ideal for testing devices with scan design built-in, it is not useful for chips without scan paths. ASIC designers who typically do not build in scan circuits are pushing a mature process technology to its limits and cannot afford to give up performance or chip size, says Daniel Skilken, product marketing manager at VLSI Technology. As a new process becomes available, designers tend to relax about speed and area since both are plentiful, he adds.

Even though the problems involved in adding scan circuits have been reduced, scan design can still add a 10% area penalty and a 3-ns gate delay to a circuit, says Skilken. But design tools are making test generation automatic for chips using scan methodology.

If a designer uses VLSI Technology's test-program generation tools, he can achieve 95% fault coverage and completely automatic test-program generation to offset what he gives up in space and performance, Skilken says. For low-volume ASICs, the cost of generating the test program in terms of man-hours can push up the per-unit cost in a big way.

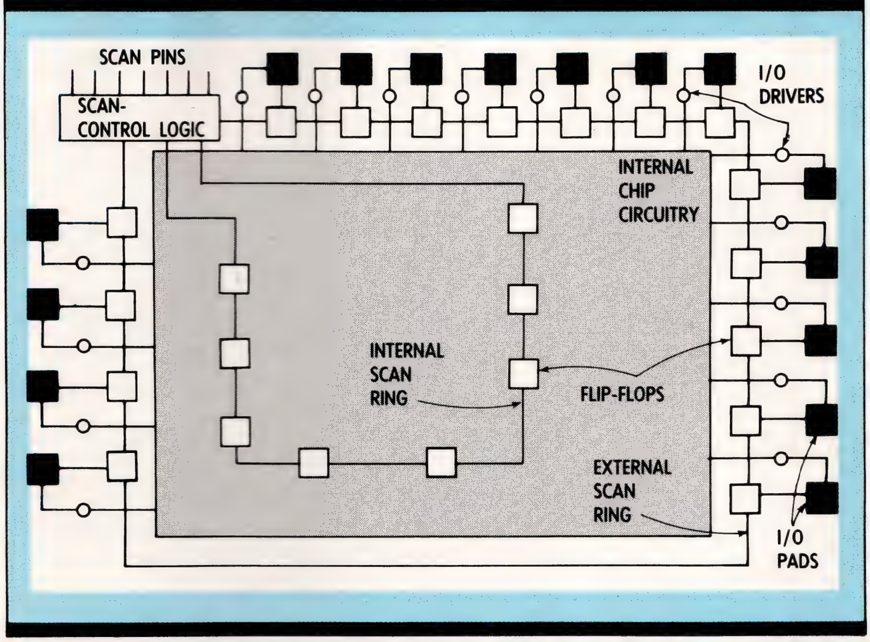
TEST GENERATION. Using VLSI Technology's tools, the designer partitions his design into functional blocks—or macrocells, functional clusters of standard cells—and generates a map showing how each block is isolated. Using the map, automatic test-generation software produces a complete test for the entire chip.

To isolate the blocks from one another, the designer adds a multiplexer on the internal connections of each functional block and ties the spare input of each multiplexer to a flip-flop in a scan ring. In this way, test patterns can be applied to the internal block from the scan-path pins. The capability is the equivalent of an in-circuit board tester isolating ICs on a board.

Once all internal blocks are tested, the program-generation software produces a functional test that checks the interconnections between the functional blocks. Other foundries can generate a test of individual internal blocks, but "we are the only foundry that has automatic test-vector generation for the entire high-level ASIC design," says Skilken.

But another scan-path advocate, Integrated CMOS Systems, has developed software that "not only generates test patterns for chips, it also generates test patterns at the board level," says Tom Miller, vice president of sales and marketing. The foundry's software tools can automatically partition a very large system-level design into ASICs and produce test patterns for chips as well as patterns for the boards these chips will occupy.

SCAN DESIGN COMES TO ASIC TESTING



The time has come, some say, to start designing testability into ASICs. One approach that's getting more attention involves adding scan paths that link a string of on-chip flip-flops.

Furthermore, the multiplexer added into the signal path adds a small amount of signal skew and pulse degradation.

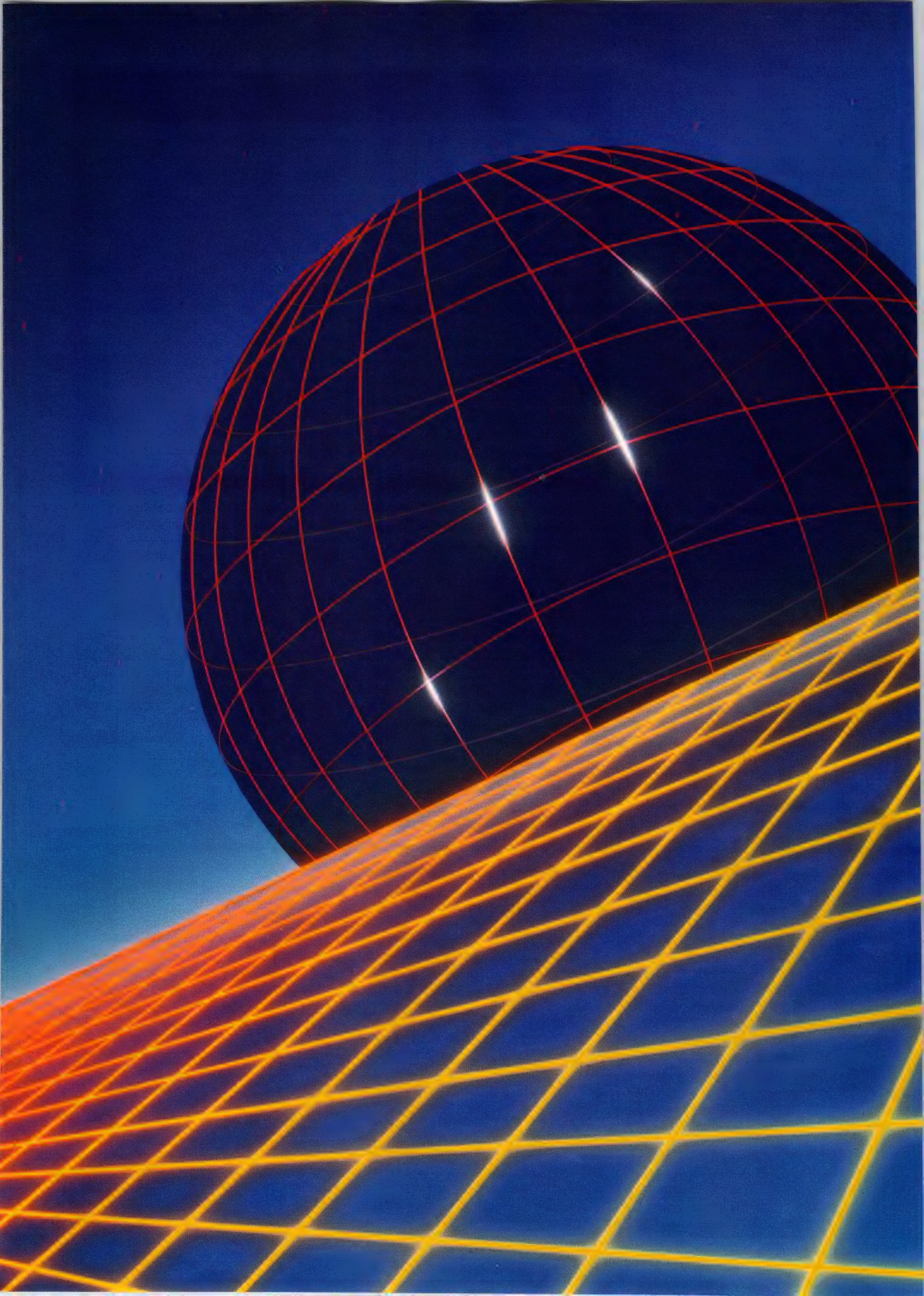
Another characteristic that sets the 82000 off from the crowd is the built-in automatic calibration feature that lets it achieve its high timing accuracy. The system's ±250-ps accuracy can be maintained for up to 30 days as long as the ambient temperature around the test system stays within ±5°C. Up to now, automatic calibration capability has been an expensive feature of expensive automatic production test system, and not commonly found on ASIC verifiers. The autocalibrating 82000 is priced at $193,000 in a 64-channel configuration.

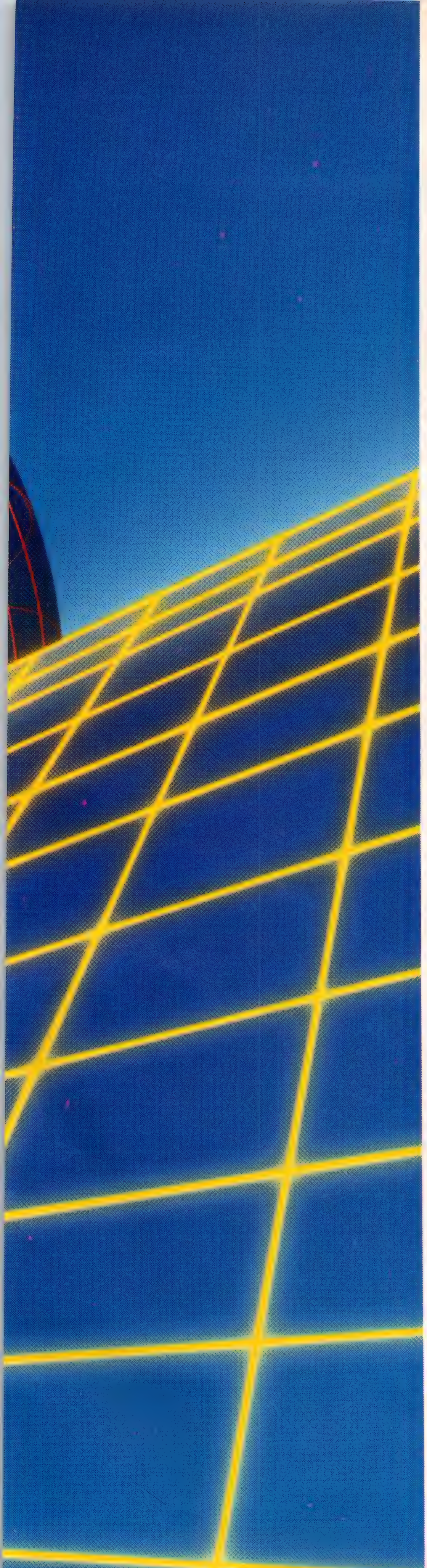
The system must be taken off-line for calibration. Calibration itself is automatic, but the operator must manually touch each pin on the test head with an active probe so that the system can make the measurements and adjust each driver/receiver card. It typically requires a few seconds to calibrate each pin. The system prompts the operator to move the probe to the next pin.

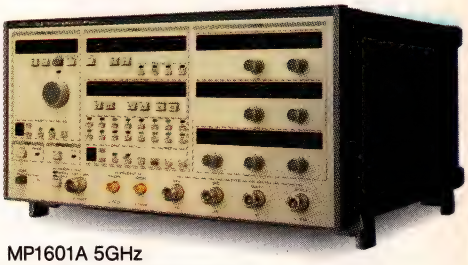
IMPEDANCE-MATCHED. This calibration process is largely responsible for the 82000's accuracy rating. But when it is used to test a chip made with ECL, accuracy is aided by the fact that the system's pin electronics has a 50-Ω pin termination right at the receiver. In testing a CMOS device that is not 50-Ω compatible, the designer must add a precision resistive interconnect to match the system and device impedance is to preserve pulse integrity.

The 82000 system's ability to handle many kinds of ASICs is enhanced by its data-format capabilities. A typical ASIC device will have different kinds of pins that require different timing formats. For example, a chip-select pin typically requires an RZ (return to zero) format; pins connecting to a data bus typically require a DNRZ (delayed nonreturn to zero) signal format; and control lines would be normally involve an NRZ (nonreturn to zero) format.

The 82000 generates these three types of signals, and two more—R1 (return to one) and RC (return to complement). Some systems provide all these formats, but only at lower data rates. They limit the number of formats at higher speeds; the 82000 offers all five formats at its full 200-MHz speed. Some ASIC-verification systems offer other formats too, such as the return-to-inhibit format. But this and other formats are seldom used, says Dave Armstrong, U. S. marketing and support manager. The five provided on the 82000 are sufficient to cover the needs of ASICs currently being designed, he says. *–J. McL.*







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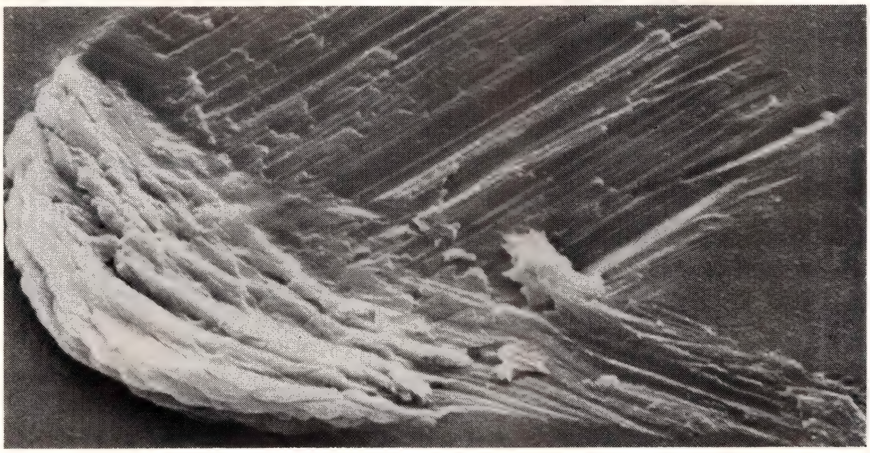


Wafer-probe testing so bad chips are not packaged cuts costs at high pin counts. But wafer probes are costly and wear out as they gouge their way through the oxide atop I/O pads (above). A new type of probe from Tektronix (below) is less abrasive and so lasts longer.

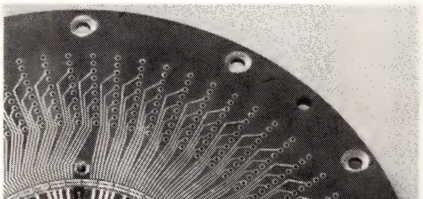
"One customer provided us with an existing design with 16 printed-circuit boards in it, a total of 450,000 gates of logic," Miller says. "We repartitioned this design into 20 ICs and automatically generated test programs for the individual chips as well as all 16 boards."

Moreover, the way Integrated CMOS Systems adds scan circuits to a chip does not degrade system performance—a major advance over previous scan-path techniques, says Miller. In addition, it adds only a 7% silicon penalty to an ASIC with 30,000 gates, he claims. To reduce the chip-area penalty, the company uses a proprietary D-type flip-flop in which the scan control is in the clock side of the flip-flop, not in a multiplexer in front of the D input. Thus, there is no additional logic in the signal path. That also means there is no degradation in system performance, he says.

But if the scan-path methodology is to be successful, new testers are needed. "Because scan-based testing is different from dc and ac parametrics test at the chip level, test equipment from ATE companies such as Advantest, Ando, Schlumberger, and others, does not address it effectively," Miller says.

What conventional ATE equipment does not provide is a large memory behind each pin to contain the long serial patterns that scan testing requires, Miller adds. Patterns for scan test are on the order of a few million bits long. A second capability the testers lack is high clock frequency to load and unload information from the chip.

The trends toward higher ASIC complexities and speeds continue to push tester makers to build systems with higher pin-count capabilities and higher data-transfer rates to satisfy the pins' appetite for test patterns. For example, the Boblingen Instrument Division in West Germany of Hewlett Packard Co., Palo Alto, Calif., has unveiled an ASIC-verification system that boasts a 200-MHz data rate (see p. 92). "The HP 82000 achieves its high data-transfer rate using technology developed for the company's counter-timer," says David Armstrong, HP's U. S. marketing and support manager.



The HP system also has automatic calibration to support the high data rate. This capability ensures that the timing accuracy, ±250 ps, and resolution, 50 ps, of the test system out to the test pins of the device under test is within specification for up to 30 days. Timing accuracy of ±500 ps and resolution of 100 ps is more typical of the specifications found on this class of ASIC verification systems, in the price range around $250,000.

Modular expandability is the accepted solution to the other side of this equation, the need to handle larger and larger pin counts. Dan Hutcheson, president of market research firm VLSI Research Inc. in San Jose, Calif., says that in 1988 there will be $6.8 million market for ICs that have 1,024 pins, $19.6 million for ICs with 512 pins or more, and $122.2 million for ICs with 256 pins or more.

Vendors of ASIC-verification systems are responding to this trend. Hewlett-Packard's 82000 can modularly expand its pin count to 384 pins. The Topaz-V ASIC verifier from HiLevel Technology Inc. of Irvine, Calif., can handle up to 320 I/O pins [*Electronics*, June 1988, p. 132].

Integrated Measurement Systems Inc. of Beaverton, Ore., has just taken pin count expansion to a new limit with its new model XL2 (see p. 97). The system boosts the number of pins the company's systems can handle from 512 up to 896 channels. The IMS XL2 will offer this high pin count at the relatively low price of $800,000.

The trend in ASIC verifiers toward high pin count for low price is being seen in full-fledged production testers as well. Gillytron's system is modularly expandable to an all-time high of 1,792 pins, for example. And Tektronix Inc. of Beaverton, Ore., will soon add a model that offers 512-pin test capability to its Vista series of VLSI test systems (see p. 101).

The growth in pin count on ASIC test systems solves the problem of testing packaged ASICs. But these high-pin-count components require costly packages. "High-pin-count packages can cost from $30 to $500," says Michael Bonham, product marketing manager for Tektronix. Chip makers want the ability to perform more thorough functional test at the wafer-test stage to save the cost of packaging bad parts. Testing at the wafer level has three problems: bringing enough I/O pins to bear, ensuring that the probe tips do not introduce errors in the test because of their low bandwidths, and the rapid wearing out of the expensive wafer probe.

These problems have not been solved by the wafer-probe offerings of the last six months. The probes on the market have a maximum pin count of around 388 pins. The maximum bandwidth of each pin is 100 MHz, insufficient to support ac timing measurements at the wafer level. A high bandwidth is desirable to ensure a square wave pulse is not elongated and rounded by the probe.

MORE TOUCHDOWNS. Conventional probe cards are of the metal-blade, ceramic-blade, and epoxy-ring varieties. During a test, the probe card contacts the wafer and breaks through the oxide coating. "Due to the mechanical stress of continuously contacting dice on each wafer, a conventional probe card is good for no more than 30,000 touchdowns," says Bonham. One reason for the wear is that conventional probe scratches the oxide coating on the I/O pads. Solving the wear problem was one of the design goals embodied in Tektronix's new P6521 probe card, pushing the figure up to 1 million touchdowns, in large part because it is far less abrasive than existing probes when it contacts the chip's I/O pads. Cer Probe Corp. of Tempe, Ariz., has also addressed this problem with a 300-pin tungsten probe that has a rated lifetime of 1 million touchdowns.

Other companies supplying probes for wafer-level test include Probe Technology Inc., a division of Micromask Inc. of Santa Clara, Calif., and Rucker & Kolls, a division of General Signal Corp. in Santa Clara, Calif. Probes from these companies sell for $12,000 to $20,000, depending on the number of pins.

The Tektronix P6521 probe card goes beyond the probe-wear question to solve the problems of higher pin count and bandwidth. It will support 360 pins initially, but the maximum will increase to 500 pins by the end of this year, and can be expanded beyond 500 pins relatively easily. To ensure high signal fidelity, the wafer probe provides a 2.5-GHz bandwidth, sufficiently high to enable test engineers to perform ac timing measurements at the wafer level for the first time.

The Tektronix probe is unique because it is fabricated using techniques similar to those used in IC manufacture. The controlled-impedance signal lines and probe tips—square pads or round bumps—are deposited on a thin-film hybrid substrate. The pattern of pads or bumps is unique to each IC family, manufacturer, die size, or pad configuration.

Although high pin count is less of a problem, there are other types of difficulties plaguing testers that target the very fastest ASICs: ECL and GaAs gate arrays. A new laser-based approach to the high-speed test problem is being brought to market by Photon Dynamics. Its System E/O "is the first to contain 20 high-speed drivers which have a data-transfer rate of 1.2 gigabits/s and 20 low-speed drivers which operate at 5 to 75 Mbits/s," says Robert Ackerman, vice president of sales for the company.

To handle fast logic, the system offers ±25-ps timing accuracy and 10-ps resolution. Another figure of merit for high speed testing is slew rate, or how fast a tester recognizes a transition from one logic state to another. The new system has a 3.3 V/ns rate. Today, high-end test systems afford a data transfer rate not much better than 300 Mbits/s, a timing accuracy of ±250 ps, and a resolution of 100 ps. And they have a slew rate of about 1.5 V/ns.

The new System E/O operates by using the high-speed drivers to apply stimulus to the input pins of a device mounted onto a special glass test fixture. A 12-by-12 array of metal dots on the fixture contact pins of the device. To measure the device response, 100-ps light pulses are directed at a metal dot contacting an output pin of the chip and are reflected back to a photodetector. Measuring the reflected light's polarization indicates the output pin's voltage. The laser samples 1 million times per second, staying with one pin for a period and then moving on. "The laser pulses operate like a sampling oscilloscope to achieve the high timing accuracy, resolution, and slew rate of the system," says Ackerman. □

MIXED LOGIC LEVELS NO PROBLEM FOR THIS TESTER

Not only are application-specific integrated circuits showing up with higher pin counts, they are also using mixed combinations of different logic levels more than ever. Systems houses that have a big appetite for these complex ASICs are as a result facing a growing problem in the area of chip verification. Now Integrated Measurements Systems Inc. is rolling out an ASIC-verification system that keeps pace with the evolving ASIC designs.

The five-year-old company has anticipated the demand for systems that meet the high-pin-count need: its new system pushes beyond the 512-pin mark now common to 896. To be available in October, the LogicMaster XL2 will perform verification on devices with 896 pins in a configuration that sells for only $800,000, says Steven Morris, product marketing manager in Beaverton, Ore. The only other systems with pin counts that high are production test systems costing more than $3 million.

In building the system, IMS added more memory for the larger test patterns required by the more complex devices. It also increased the number of timing edges and the number of drive levels any one pin could produce to handle the variety of logic families—CMOS and ECL with varying characteristics—that are likely on more complex ASICs and hybrids. The company's earlier system supported 24 timing edges; the XL2 doubles that number.

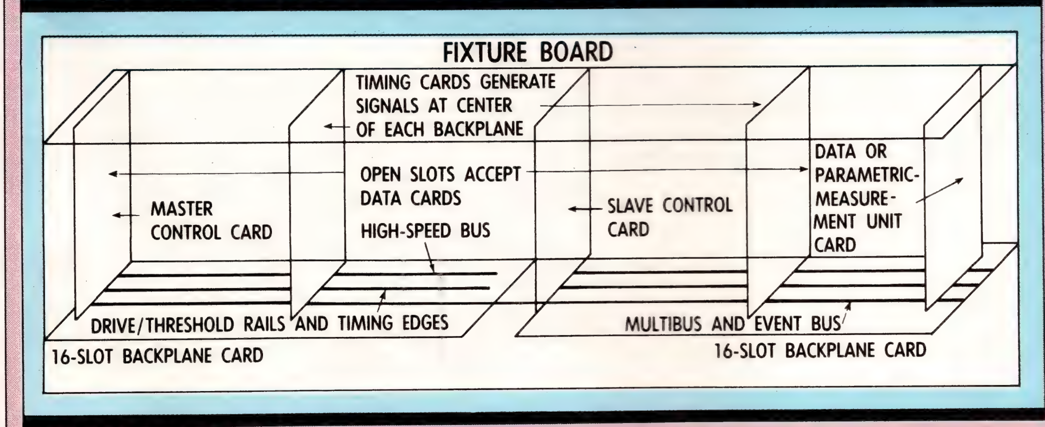
NICHE. ASIC verification is a growing market opportunity, points out Deborah Matsuhiro, an analyst at VLSI Research Inc. in San Jose, Calif. The company says the market will see a compound annual growth rate of 22.6% through 1992. "The market was worth $42.7 million in 1987 and will be $118 million in 1992," she predicts. From this total the portion of the market that is demanding high-pin-count capability is on the order of 10%, says Morris. That translates into $12 million in 1992, a good piece of business for a market containing only a handful of small competitors.

The XL2 system developed by IMS supports up to 64 Kbits of memory behind each pin. In addition, there are pattern-compression capabilities built into the system to accommodate even longer patterns. The XL2 system is also set up for looping on a vector or set of vectors any number of times. Thus, the system can stimulate a device with hundreds of thousands or millions of vectors without having the need to reload patterns.

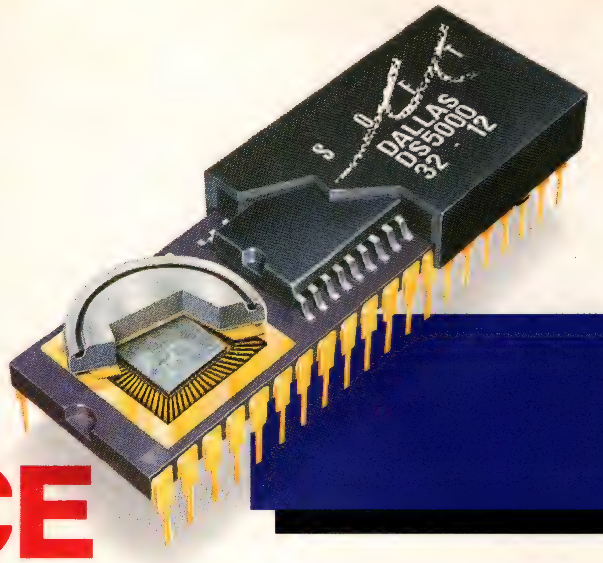
To get so much memory behind so many pins, the XL2 has been designed with a dual-backplane system architecture that can accommodate 25 data cards, two power cards, and a parametric-measurement-unit card. To maintain timing accuracy in a system with so many cards, it has been set up so that no data card is more than seven slots distant from the source of its timing-edge signals.

In addition, the XL2 doubles the number of different drive rails to eight, from four in earlier version systems. That allows the system to provide voltage levels for "four different types of technologies: TTL, CMOS, ECL, and one other type of technology," says Morris. This capability is especially useful for testing large hybrids containing a mix of different device technologies. *–J. McL.*

ONE ANSWER TO HIGH-PIN-COUNT ASICs


FIXTURE BOARD
TIMING CARDS GENERATE SIGNALS AT CENTER OF EACH BACKPLANE
OPEN SLOTS ACCEPT DATA CARDS
MASTER CONTROL CARD
HIGH-SPEED BUS
SLAVE CONTROL CARD
DATA OR PARAMETRIC-MEASUREMENT UNIT CARD
DRIVE/THRESHOLD RAILS AND TIMING EDGES
MULTIBUS AND EVENT BUS
16-SLOT BACKPLANE CARD
16-SLOT BACKPLANE CARD

To test 896-pin ASICs, IMS developed a dual-backplane design for its XL2 ASIC-verification system that lets users add data cards up to a maximum of 28, and set it up so that all cards are near a source of timing signals.



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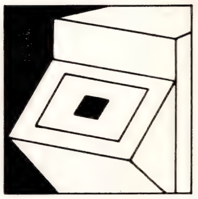
GILLYTRON'S SCAN-PATH TESTER IS RIGHT ON TIME

The modularly expandable test system can match the soaring pin-count demands of ASIC chips and its fault coverage is nearly 100%



Application-specific integrated circuits are getting very complex, many of them far more complex than any but a handful of standard VLSI parts. The testing problem for big, high-pin-count ASICs is getting way out of hand too, and the approach of throwing more and more expensive tester horsepower and testing time at the chips is not going to take the industry much farther. Bold moves must be taken—radical steps like the scan-path approach being promoted by a newcomer to the ASIC-test field, Gillytron Inc. of San Jose, Calif., and its development partner, ASIC-vendor Integrated CMOS Systems Inc. of Sunnyvale, Calif.

The basic concept of level-sensitive scan design, in which loops of serially connected flip-flops are added to a chip's circuitry for testing purposes, was developed over a decade ago. But the concept has seen only limited use due to its drawbacks: making the chip larger, and thus more expensive, and slowing it down somewhat because the added test circuits placed some load on the active circuits. But the founders of Gillytron are betting their young company—scan-path testing is Gillytron's only business—on the perception that improvements in scan-path techniques and the soaring testing demands of ASIC chips will bring scan design into wide use very soon.

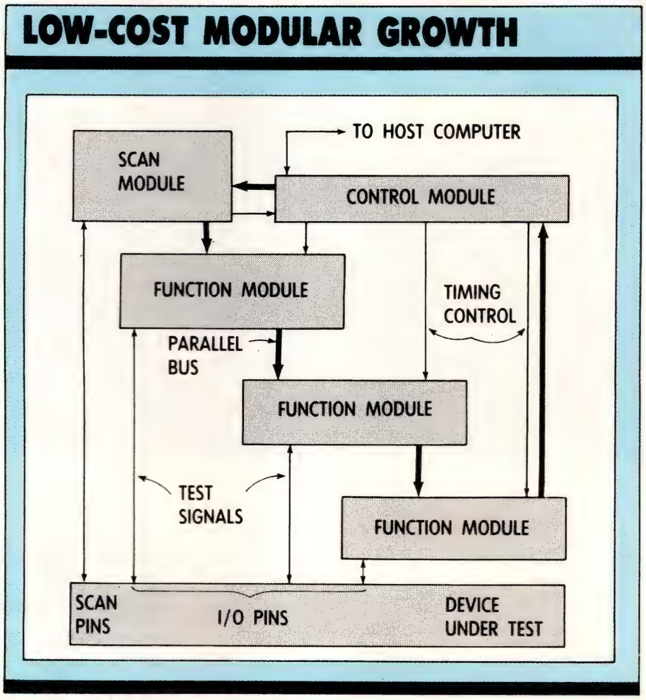
Gillytron's new tester, the ScanMaster DV-8005, is designed to test chips with built-in scan paths. The modularly expandable system offers a cost-effective solution for large ASICs—up to 1,792 pins—but cannot be used to test chips that do not contain scan paths. Through the scan methodology, the system can make a more thorough test of a chip than a conventional test system, approaching 100% fault coverage thanks to its access to nodes inside the chip via the scan paths. It can also check the chip's ac characteristics by running the internal scan paths as ring oscillators and seeing how fast they can clock before they start malfunctioning.

The complexity of run-of-the-mill ASICs is now reaching well over 10,000 gates and the number of input/output pins can be as high as 512. Users can buy expensive testers with more channels, higher clock frequencies, and more complex pattern-generation capability. But with production testers running more than $1 million each, chip and board makers are beginning to open up to solutions that didn't make sense to them one or two years ago.

If a company designing an ASIC is willing to make the move to synchronous design techniques and built-in scan paths, Gillytron's ScanMaster solution can guarantee a much lower cost for testing a device. A system with 512-pin test capability sells for $512,000, one quarter the price of a conventional high-end automatic test system with 512 channels. The Gillytron system can also be used for testing at the board level, once the move to scan design is made.

Gillytron's system provides nearly 100% fault coverage and completely automatic test program generation. With conventional testers, 85% fault coverage is considered high and though stimulus patterns from a logic simulator can be used in the test system, manual pattern generation is often required to boost fault coverage.

LOW-COST MODULAR GROWTH



By daisychaining function modules, a user of Gillytron's ScanMaster DV-8005 can configure a system with up 1,792 channels.

Integrated CMOS Systems, for example, says it hit 99% fault coverage on 10 gate arrays with more than 30,000 gates each. The arrays were designed for the DN 10000 work station from Apollo Computer Inc. of Chelmsford, Mass. And the ASIC foundry says that its scan circuits had no impact on chip speed and required only a 7% real-estate penalty.

Automatic test-program generation tools developed by Integrated CMOS Systems not only add the scan circuits to the design automatically but also produce the test patterns. The software generates the patterns needed to apply to the I/O pins, the serial data to be serially shifted into the chip via the scan data lines, and the known-good patterns to check the chip's responses against.

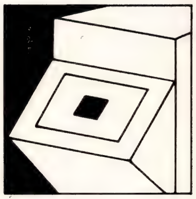
DIRECT TRANSFER. The test-pattern data can be transferred directly to Gillytron's system. Available now, the DV-8005 comes with a PC-AT-compatible user console, a 68020-based control module, up to four 68020-based scan modules, and up to 14 function modules, each with 128 channels, for a potential of 1,792. Scan modules provide 23 clock and control lines for the scan circuits embedded in the device and scan-data-in and -out lines.

The tester performs a functional test to ensure that every node works, a ring-oscillator test to ensure that the chip functions up to its ac specification, and a dc parametric test of every pin on the chip to ensure the chip meets its dc specifications. The scan circuits add a degree of visibility inside the chip not possible without them. Any logic circuit inside the chip containing a flip-flop can be accessed via the scan paths. For example, an adder circuit can be checked completely even if its outputs are not directly accessible from the I/O pins.

Using scan paths, circuit nodes can be accessed and checked for stuck-at faults. But this test stage does not check the circuit at speed. The parallel patterns applied via the I/O pins are clocked at a 5-MHz data rate, and serial data from the scan module is shifted in and out at 10 MHz.

To check a device's ac performance, the entire internal scan ring is run as a ring oscillator at a frequency selectable from 2 kHz to 100 MHz with ±0.1% accuracy. If a circuit path does not propagate properly to meet the setup and hold times for a particular flip-flop, it will be reflected as a stuck-at fault. The ability to check circuits at up to 100 MHz means the tester can handle the fastest ECL and GaAs logic. If the circuit oscillates at a frequency predicted by the simulator, the user can be sure the chip will run at full speed. *–J.McL.*

HOW TEKTRONIX IS USING ASICs TO TEST ASICs



The ultimate hat trick in the competitive field of automatic test equipment for dense integrated circuits is to offer ATE for high-pin-count ICs, high pattern-generation rates, and high degrees of accuracy without pushing the price tag into the stratosphere. Such leading-edge ATE systems typically cost about $3.5 million, but Tektronix Inc. is now pulling together all three of those testing features in systems priced at $1.6 million—quite a trick indeed.

The Beaverton, Ore., company is reaching those marks using a mixed bag of semiconductor technology that employs a unique die-temperature feedback loop for accuracy; a modular ATE system architecture; and a unique software-based calibration system that promises to maintain testing accuracy up to two months at a shot. The result is the latest members of Tektronix's Vista series of testers, the LT-1100 and the LT-1100+, which debuts this month. The two new systems take maximum-pin-count testing for very large-scale ICs to 512 leads (double Vista's previous ceiling). The 1100+ system cranks up the systems' speed, doubling the clock rate to 200 Mbits/s.

READY FOR 200 MHz. The move to introduce high-pin-count VLSI testers is being made in anticipation of the next wave of faster, highly complex chips—particularly semicustom application-specific ICs, which Tektronix managers say will hit the 512-pin count by 1990. By then, they believe, ASIC devices will have clock rates of 100 MHz. With two unique ASIC chips on its own test-pin handling boards, the 1100+ is even ready for 200-MHz clock speeds. And Tektronix's semiconductor test system division is planning future Vista generations for mixed analog-digital signal testing.

Key to the continuing expansion of the Vista series is a highly modular system architecture that can handle increasingly complex ICs with additional system cards. "We designed the product to address a pin count from 32 pins all the way up to 2,000 pins," says Michael J. Kondrat, the division's marketing manager. "That allows us to increase the pin count without redesigning the system from one tester generation to the next."

In addition, Tektronix is using ASICs to boost ASIC testing. "We have integrated the driver-comparator pin electronics into two 1.2-μm CMOS ASICs," says Kondrat. "We put all the edge generation, formatting, and comparison capability for signals, clock, and pattern data that must be fed into each test pin in the two ASICs."

With that level of silicon integration, eight driver-comparators can reside on a single pin-electronics card, which can be placed within three inches of the device pin. The shorter connections to the chip under test mean higher data rates and increased accuracy.

In contrast to the ASIC approach, other test makers use high-power-dissipating bipolar gate arrays and hybrid circuits to handle the pin electronics and are forced to multiplex pin electronics on the pins of the tested device. Kondrat says both take up more space, cost more to implement, and consume much more power than the ASIC solution. What's more, they are limited in the density of the chips they can test: by using two pin-electronics resources per pin, only 256-pin ICs can be tested at 200-Mbits/s, rather than the 512 of the Tektronix systems, says Kondrat. He adds that performance of the firm's 1.2-μm CMOS ASICs is comparable to the typically used bipolar parts.

Special ASICs in tester use on-chip feedback loop to control their own temperature

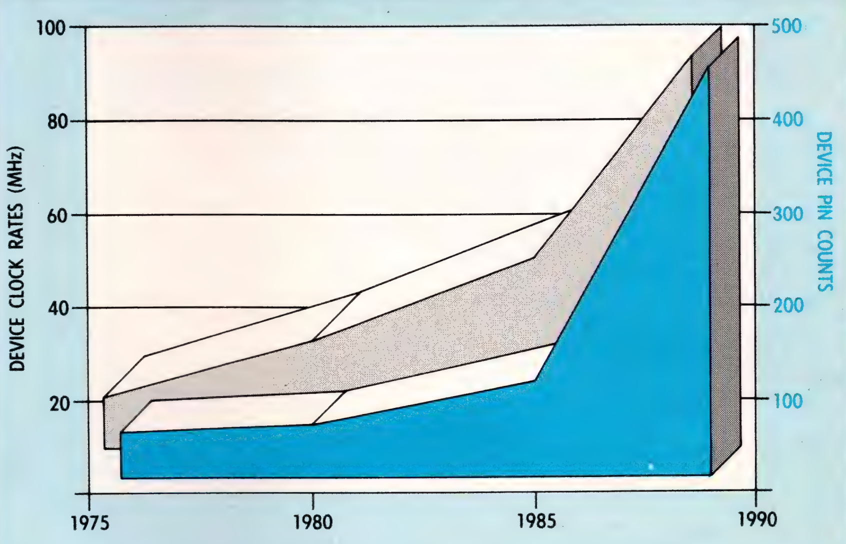
There is, however, one drawback to the ASIC scheme: using CMOS devices in test systems means that characteristics change with temperature variations. To get around this, Tektronix has developed a patented technique for temperature compensation in its ASICs. The technique employs a feedback loop on-chip to heat the die to a known and constant level. The temperature-controlling feedback loop is similar to one used by Tektronix on analog parts in its spectrum analyzers.

The new testers have programming timing resolutions of 39 ps and a ±275 ps accuracy rating, the latter due to a software-imposed accuracy feature—software calibration. An external calibration system measures all the signals in the test head, determining the error margin of each pin on the test head's pin card. This error setting is then stored in the ASIC driver-comparator ICs as a compensation value. The devices use it to take into account clock errors, cabling errors, process errors in the ICs, fixture errors, and any other errors.

"We calibrate a system once per month, and we are looking at increasing this interval to every six or eight weeks, because of the stability of the circuits once they have been calibrated," Kondrat says. "The calibration enables the test system to produce repeatable results within 50 ps." The software approach lets Tektronix avoid the higher costs of making "precise CMOS devices and incurring the expense of this manufacturing process," Kondrat notes.

The Vista series calibration source, which consists of a counter and voltmeter, is wheeled to the system being set and placed in automatic mode. It can serve more than one tester, providing corrrelation between systems. *–J. McL.*

TESTERS FACE A STEEP CHALLENGE



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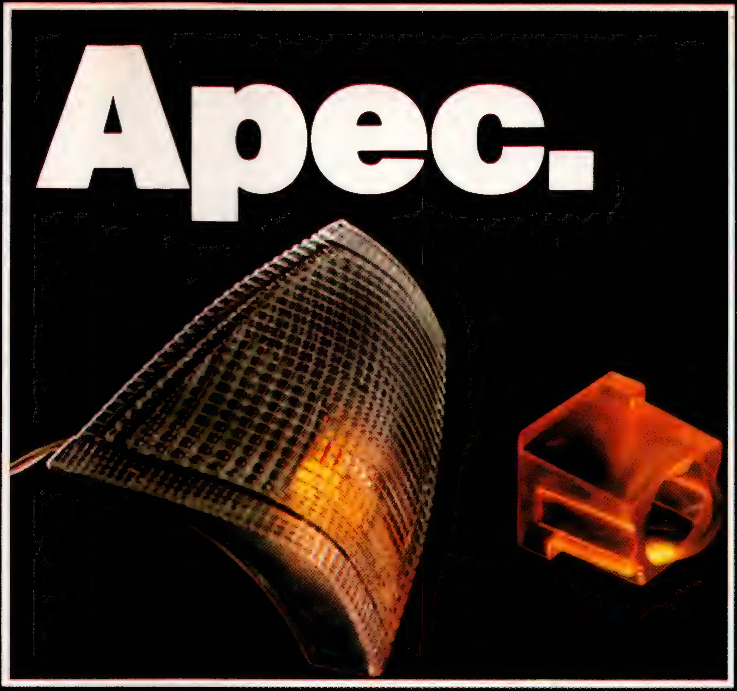

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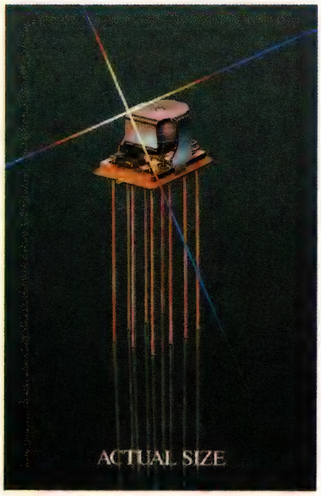

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CAN ELECTRONICS MANUFACTURERS BANK ON SUPERCONDUCTIVITY?

U. S-Japan competition is fanning R&D fires, but there's no sign yet of the needed breakthroughs

by Samuel Weber

Superconductivity at relatively high temperatures may have disappeared from the headlines, but those recent laboratory discoveries have set off an international contest for technological dominance of the new field. The U. S. and Japan are leading the way, with heavy investments by big industry, venture-backed startups, and government in fundamental research.

At stake is leadership in a worldwide market that some say could zoom from almost nothing today to $20 billion by the year 2000. But there are some tremendous barriers to overcome before practical applications appear—the new high-temperature superconducting materials are not even completely understood at this point. In fact, some observers question whether the breakthrough will ultimately amount to anything, at least in electronics applications.

There is no doubt that the materials, which won IBM Corp. researchers J. Georg Bednarz and Karl Alex Müller the Nobel Prize, have launched a host of research and development drives that hope to tame high-temperature superconductive materials for practical use. In the U. S., there are already several startup companies, a handful of large companies with major R&D programs under way, and a few universities with government-supported R&D programs. An aggressive national program in Japan, however, has once again invoked the specter of the U. S. falling behind in an important technology (see p. 109).

PAYOFF. Failure to encourage or nurture the technology's development, called high-temperature superconductivity, or HTS, could be disastrous for the U. S., some observers say. And those who support continued or even escalated R&D efforts say there will be a huge commercial payoff. A lot of the speculation is fueled by proposals for magnetically levitated trains, power transmission without loss, highly efficient rotating machinery, and electromagnetic weapon-launching systems.

For now, progress in using superconducting materials in electronics applications is barely measurable. Enthusiasts have proposed using the technology in superconducting interconnects and high-speed digital elements for supercomputers; in low-loss microwave-resonant structures for ultrastable oscillators and antenna elements; in ultrasensitive magnetic and infrared sensor arrays for medical and military/aerospace systems; and in electromagnetic shielding for electronic systems.

But the payoff in marvelous new applications now trumpeted in the media is far off at best, argue some observers. These cautionary voices say the field has enough support, at least until ongoing research hits more pay dirt. Another criticism is that even if practical electronic devices that can operate at liquid nitrogen temperatures or higher become reality, little will be gained if they are merely replacements for existing devices. High-temperature superconductivity will have to bring something to the party besides marginal improvements in performance to justify the necessary investment, they say.

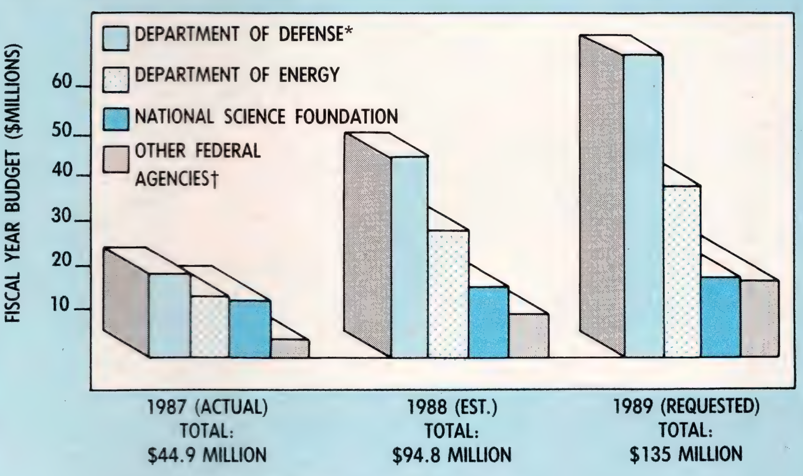
As researchers struggle to improve the brittle and environmentally sensitive ceramic materials (see p. 111), there is doubt about their potential in the near future for electronics. Even Harry Kroger, director of the superconductor program at Microelectronics and Computer Technology Corp. in Austin, says: "Widows and orphans shouldn't invest in HTS."

Others warn that electronics applications are simply being overstated. "I believe in good science, and this represents a real breakthrough," says George Heilmeier, senior vice president and chief scientific officer of Texas Instruments Inc. in Dallas. "But a lot of the claims for high-temperature superconductivity to date are just so much arm-waving. They talk about superconducting infrared sensor arrays, but these are already limited by background noise. How is superconductivity going to improve their performance?

"The same is true for very sensitive magnetometers from the standpoint of military systems. Under special circumstances, there might be advantages in interconnects at the board level, but then you bring along a lot of other problems.

EXECUTIVE BRIEFING is a monthly feature of Electronics *that provides managers with a concise review of developments in fields that are making frequent headlines.*

THE U.S. R&D COMMITMENT BUILDS



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Circle 107 on reader service card

If you're interested in board-to-board communications, you have to look at the tradeoffs. An optical link between boards might be a better way to do it."

There are also difficulties in designing circuits without a gain element, says Heilmeier. "Whenever I raise these issues in 'mixed company,' they look at me as though I've said a four-letter word in church," he says wryly.

HYBRIDS. But another widely held view is that success for high-temperature superconductivity does not lie only in simply replacing existing electronic functions. Kroger, who is directing a 13-member cooperative research program, says, "If you replace copper with superconductors you can get improvement, but it wouldn't be a world-beater. Yet there may be application areas where you can do something you couldn't do before. We've looked at a number of things in hybrids, for example, where you can combine semiconductor devices with superconductor devices, where you want to do something that neither technology can do by itself."

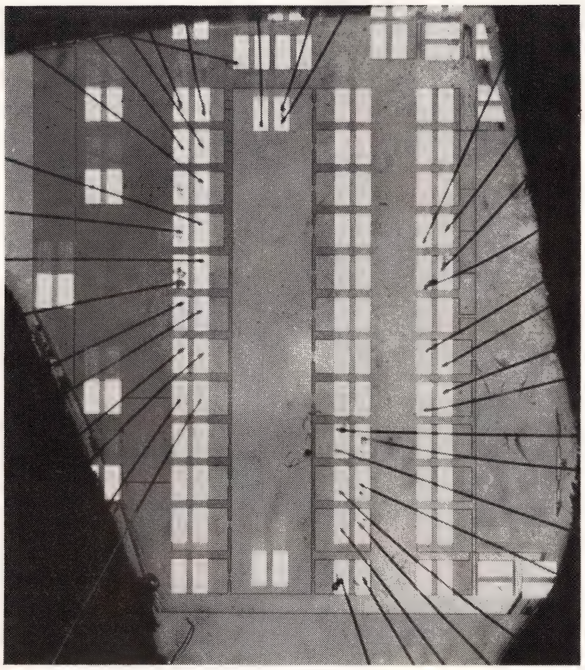
Giving mixed reviews of the technology's potential is Henry Kressel, a former scientist and now a venture capitalist at E. M. Warburg, Pincus Inc. in New York. Many people are pursuing superconductor work without stopping to figure out how they will apply it, he says. "So far, none of the new materials represents a replacement for the known art in superconductivity," Kressel says. "You can invest a lot of money in speculative things like superconductivity, but you could end up doing at 77 K what you could do at 10 K. It's easier and cheaper to refrigerate at 77 K than at 10 K, but you had better define your applications."

Kressel has put his company's venture capital into Hypres Inc., Elmsford, N. Y., a firm that was first to develop a commercial instrument using low-temperature superconductive devices with niobium Josephson junction devices as a base [*Electronics,* Feb. 19, 1987, p. 49].

But he says the future of high-temperature superconductivity also holds promise. "The encouraging thing in this development is that it shows that there exist in nature many materials that superconduct. People are poking around. They may discover materials that have more desirable properties than the current ones. We just don't know what the limits are."

Kressel's optimism gets a strong second from Lawrence Murr, president and chief executive officer of Monolithic Semiconductors Inc., a Lake Oswego, Ore., startup. "The most exciting things that we can do with these materials haven't even been thought of yet," he says. "People have been caught in a trap. They're trying to go traditional routes with a material that's completely uncooperative. It just isn't going to go in that direction."

But the fact remains that no one has yet built a practical, functioning electronic device with high-temperature superconductivity. Electronic functions have only been achieved using two-terminal Josephson-junction devices, which exhibit no gain and are unsatisfactory as memory devices. So far, the three-terminal superconducting device is "out to lunch," says TI's Heilmeier.



IBM has built superconducting ICs containing weak-link Squids using a thin film laid on a strontium titanate substrate.

It's no wonder that many diverging opinions exist about the technology's potential, because the field of superconductivity has been, and continues to be, a complex exploration of new and still-mysterious materials. Although venture capitalists are now bankrolling a bevy of startups in the U. S., most new companies have been spawned by universities, and are still in the research and development stage. In addition, despite the Reagan administration's great show of interest and support, budgetary restrictions and a lack of nurturing legislation have curtailed the commercialization of superconductivity intended for nondefense-related development.

HUGE MARKET. But if the drawbacks of the primarily ceramic materials can be overcome—they're difficult to manufacture in a usable and consistent form—excitement persists over the market that could result. While the idea of materials that function at room temperatures still appears far-fetched, the market projections might indeed be huge if research progresses to that point.

One of the new startup companies, American Superconductor Corp., Cambridge, Mass., estimates that the total annual U. S. market for superconductors will exceed $100 million by 1990, $1 billion by 1995, and $5 billion by the year 2000. Glenn E. Penisten, a general partner in Alpha Partners, a Menlo Park, Calif., venture capital firm, believes there will be at least 25 superconductor startups by the mid-1990s, and that one or two of them will have more than $1 billion in annual sales. Penisten, formerly chief executive officer of American Microsystems Inc., has helped found one startup—Superconductor Technologies Inc. of Santa Barbara, Calif., where he served as president and CEO until recently.

Even more optimistic in projections are the Japanese, who have taken "a great leap of faith" in the words of one U. S. observer. In a survey taken a year ago, 60% of 167 Japanese companies that responded expected a worldwide superconductor market of $20 billion by the year 2000. Although not all of this, by any means, is in electronics markets, most of the respondents listed electronics as the most promising area.

And the Japanese are sweating to realize their expectations, says the U. S. Office of Technology Assessment in a recent report. The report warns that commitments in Japan substantially exceed those in the U. S. Firms in Japan have 900 employees in industry assigned to superconductivity; U. S. companies have 625. What's more, Japanese industrial firms budgeted $90 million for superconducting R&D, while total Japanese government and industrial spending for 1988 should exceed $160 million, the OTA report says. And the Japanese are not just operating in an R&D mode. They are thinking about applications and manufacturing right off the bat.

At first glance, the U. S. is spending more on high-temperature superconductor R&D than Japan, with government agencies budgeted to spend $95 million in fiscal year 1988. Also, 55 U. S. firms report that they will spend about $97 million (on low- as well as high-temperature superconductivity). But nearly half the U. S funds are going to the DOD for military projects. In addition, most of the government funding represents little new money; quite a bit has been diverted from other projects. And recently there was a temporary freeze on DOD funds, just now restored at 75% of the previous level.

The Department of Energy also accounts for much superconductor research in the U. S. It has set up superconducting pilot centers at Los Alamos, Argonne, and Oak Ridge national laboratories. As a result of President Reagan's Superconductivity Initiative, announced in July 1987, many other federal laboratories have set up technology transfer programs to speed the dissemination of research information on superconductors. But the history of technology transfer out of these laboratories is not encouraging. One director of an industrial superconductor R&D program, who asked not to be identified, says, "A lot of money being spent by DOE is not going to result in commercialization no matter how many work centers there are. The national labs spent lots of money that never helped American competitiveness. It's extremely difficult to do technology transfer when you've spent your life doing nothing but pure research. And that's more or less what scientists at the national labs are like."

FUNDAMENTAL WORK. The National Science Foundation supports research in the nation's universities, where much of the valuable fundamental superconductor work has already been done. With relatively few large companies having aggressive superconductor R&D programs, most of the preliminary commercialization work will have to be done in universities. Although the NSF plans to spend $14.5 million in fiscal 1988, it receives many more highly rated proposals for projects than it has the funds to underwrite, according to its administrators.

Over a year ago, the Defense Advanced Research Projects Agency, in conjunction with the Office of Naval Research, solicited proposals from industry for the development of processing techniques for superconducting materials aimed at real applications. More than 200 came in. Darpa accepted proposals from 16 companies and 4 universities for negotiations, but the temporary DOD freeze on all R&D funds kept them from awarding almost all the contracts until a thaw in July 1988 permitted some to proceed with reduced funds.

Whether agencies will be able to proceed with technology transfer programs is just one question. Perhaps the primary obstacle to using high-temperature superconductors is the lack of a basic theory explaining their behavior. "We're getting closer," says Alexis P. Malozemoff, coordinator for high-temperature superconductivity at IBM Corp.'s research division in Yorktown Heights, N. Y. "But in my opinion there is no convergence yet on what the underlying mechanism is. One problem is that the key experimental data needed to resolve these questions is just coming in. In fact, many basic facts are being revised from the early studies that were done in some haste."

Often the initial interpretations were considered sensible in the perspective of "old-fashioned" superconductivity, he says. However, in the context of the new superconductivity, "we're realizing that many phenomena are just plain new and different and have to be looked at in a new and different way."

Malozemoff cites as one example the recent discovery at IBM of a new phenomenon called giant flux creep. It might turn out to be a fundamental limitation in the quest for room-temperature superconductors. Studies of a basic property of the materials called coherence length—the distance between the paired electrons that are characteristic of superconductive materials—involve measurements of the upper critical magnetic field. "People have generated all kinds of data showing that as you apply a field, the temperature shifts downward," the IBM researcher says. "We discovered that these measurements were not actually measuring the upper critical field, but something new

JAPAN'S NEXT TARGET: SUPERCONDUCTORS

Japan's big move in high-temperature superconductivity, with two government agencies leading the way, includes a superconductivity center that will open in October near Tokyo, generous funding for present research and development efforts, and a forthcoming 10-year project. This all-out effort is causing a lot of alarm in the U. S.

Those fears aren't being quelled by Japan's creation of the International Superconductivity Technology Center, which is accepting non-Japanese concerns as members. In fact, no U. S. subsidiaries in Japan have chosen to be full members.

The center was set up as an international organization to help avoid the friction between the U. S. and Japan that developed in the semiconductor industry, says Takashi Askutsu, senior managing director. The 10-year program is the first joint basic-research effort in Japan and the first open to non-Japanese companies. Industries represented include electronics, electric power, cable, iron and steel, automobiles, metals, chemicals, and banking.

Will the three-pronged effort vault Japan into a lead over the U. S.?

The center has two membership categories: B-level members actively participate in research and must contribute $770,000 initially and another $7,700 each year. They members will have immediate access to research results. The A-level members only have access to publications and symposia for a $7,700 tab to join and $150 each year.

PATENT RIGHTS. Of the 100 member firms, 45 are in the B-level category. Subsidiaries of U. S.-based firms such as Du-Pont, Rockwell, and IBM have only become A-level members, which is a disappointment, says Askutsu. The reluctance of U. S. firms to join fully may be due to the not-quite-clear ownership of intellectual property rights and patents arising from the research.

But a lot is happening in high-temperature superconductivity in Japan in addition to the center's plans. The Ministry of International Trade and Industry and the Science & Technology Agency provide almost 90% of the 1988 funding for government-sponsored programs. The STA's superconductivity efforts utilize a decentralized approach that involves nine laboratories and other government organizations working on theory, materials, processing, and technology transfer. Other major programs using STA funds are under way at the National Institute for Research on Inorganic Materials and the Atomic Energy Research Institute.

Another major Japanese effort, scheduled to be launched in October, will be a 10-year superconductor project, sponsored by a subagency of the MITI. The project will support work done at government laboratories and pay for contract research. Its two areas of concentration will be superconducting materials and superconducting devices.

Appropriations for fiscal 1988 extending through March 1989 add up to $5.25 million for materials and $3 million for device work. Of this, contract research will be $3.5 million for materials and $23,000 for devices. Industry sources estimate total funding for the 10-year period will be about $77 million for materials research and $44 million for device research.

The research efforts planned by Japanese government agencies are worrying some U. S. observers. Stanley R. Rich, publisher of the monthly newsletter *Cambridge Report on Superconductivity,* says what has been reported about Japanese plans underestimates its true commitment to the technology. He warns of a possibly widening gap between Japan and the U. S. in superconductive know-how.

Rich is not the only one concerned. Other observers are nervous as well, and as a result they have formed the Council on Superconductivity for American Competitiveness. The Washington-based organization's membership includes corporations, government officials, and university researchers. The council founder is George A. Keyworth II, the former science adviser to President Reagan and now director of research at the Hudson Institute. *–Charles L. Cohen* that is simply not present in conventional superconductivity.

"In these materials," he adds, "magnetic fields penetrate in the form of vortices that get 'pinned' in various imperfections in the material." When current is sent through the material, the electromagnetic forces created tend to force the vortices out of these pinning centers. If the barriers are sufficiently high, the flux won't move, and there is no dissipation. But ironically, as the material gets purer with fewer defects, there is less pinning, the flux moves, and the result is more and more dissipation. "So this phenomenon of flux creep now dominates a lot of properties," says Malozemoff. "You think you're measuring one thing but you're really measuring this flux-hopping."

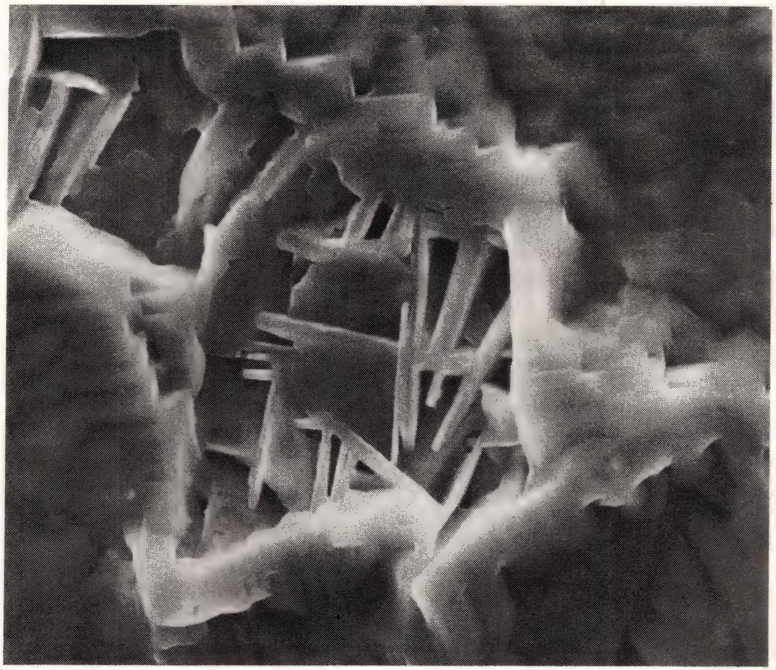
The researchers at IBM, like many others, are exploring the behavior of grain boundaries within the superconductive materials, because it is at the boundary that current is most severely affected. "We would prefer to have the flexibility to put the material down in polycrystalline form, rather than epitaxially," Malozemoff says. "For complex electronic applications, you want to be able to use this material as interconnect lines put down on top of an insulator or with different layers of metals, as in a hybrid system. Understanding grain boundaries and polycrystalline material is absolutely vital, and we're making a great deal of progress."

IBM researchers have developed a way to make very large isolated grain boundaries, build structures on top of them, and make measurements on individual grain boundaries. The company found that a single grain boundary exhibits properties similar to Josephson junction elements. Although attempts to build Josephson junction devices with these elements have failed, Malozemoff deems their presence a very exciting development.

Studies headed by Robert Laibowitz, a member of IBM's technical staff in Yorktown Heights, are investigating the properties of superconductive thin films. The research involves materials formed from a mixture of yttrium and barium in a copper oxide (YBCO). The laboratory is exploring ways of producing and patterning the films using such techniques as electron beam evaporation, sputtering, molecular beam epitaxy, CVD, and laser ablation.

The laboratory has produced some of the first high-temperature superconducting quantum interference devices from YBCO films that were epitaxially deposited on a strontium titanate substrate (see photo p. 108). These magnetic sensors, operating at 77 K, are an order of magnitude less sensitive than low-temperature superconducting counterparts that operate at liquid helium temperatures.

IBM's Almaden Research Laboratory achieved the record for zero-resistance superconductivity with thallium barium calcium copper oxide, at 120 K. Current densities are promising but there's a lot of work to be done "to get the chemistry under control," says Malozemoff. The materials are multiphased, and thin-film samples are just becoming available.



Needlelike structures emerge from the granular material in a high-current-density melt-textured superconducting compound developed at Bell Laboratories.

Another company with a large research program devoted to superconducting is AT&T Bell Laboratories, and the Bell researchers have made many important contributions to the burgeoning field. Two recent developments include a melt-processing technique, which produces bulk forms of YBCO materials that exhibit much higher critical current densities (7,400 A/cm^2) than heretofore realized with conventional sintered materials. The other was the discovery of a 30 K superconductor that contains no copper—previously thought to be essential for high-temperature superconducting materials.

Bob Dynes, director of chemical physics research at Bell Labs, is enthusiastic about the potential of superconductivity, while carefully pointing out the long-term nature of the technology. "This is a whole new class of materials which we didn't know existed," he says. "We now know that with very subtle changes, you can take a piece of this stuff, and by suitably baking it, damaging it, ion-implanting it, or otherwise processing it using known techniques, you can vary this material from a superconductor to an insulator to a magnet and everything in between."

E. I. DuPont De Nemours & Co. is another large U. S. industrial firm that has mounted a substantial R&D effort in superconductivity, with a budget between $9 and $12 million and a staff of 30. Edward Mead, director of business development, says the company is not interested in being in the superconductor materials business. "We want to grow higher value-added electronic businesses and develop devices, and even systems, with superconductive materials," he explains. Because of DuPont's history as a leader in the manufacture of thick-film pastes, Mead says there could be an opportunity in hybrid circuits using superconducting thick films.

Applications are probably years away, but the company is in it "for the long pull," Mead says. DuPont executives are already starting to think about products and have established a product concept center, staffed by eight technical professionals, to develop value-added products. "We'll be willing to form alliances with systems companies or device makers who can use what we develop," Mead adds.

In addition to the few large companies with major R&D projects, much of the innovative work is coming from startups. Executives at these startups are drawing comparisons between nascent superconductor technology and the fiber-optic or laser industries when they were in their infancy.

STARTUPS. One of the startups is American Superconductor, a company that is pinning its hopes on superconductivity emerging as the technology of the future. American Superconductor uses two techniques to produce high-temperature oxide superconductors—a metal and a polymer precursor process. These oxides become superconducting at temperatures of 36 K and above.

The firm was formed by four Massachusetts Institute of Technology professors in April 1987, with seed money provided by American Research & Development Inc., Boston, and Rothschild Ventures in New York City. Since then, the company has received $4.35 million in venture capital from backers that include Kleiner, Perkins, Caufield & Byers, Venrock Associates, and MIT.

By the middle of 1989, American Superconductor should be producing "significant samples" of both its microcable and thin-film superconductors, says George McKinney III, the company's acting president and a general partner in American Research & Development. In addition, the firm should be ready to announce joint development agreements with partners having both expertise in specific superconductor applications and funds to support major development programs, he says.

American Superconductor's processes stem from MIT patents for which it is the exclusive licensee, says Gregory Yurek, one of the founders, who recently became the company's full-time vice president for research. The company's primary focus is to produce superconducting microcable using a metal-precursor technique; a polymer-precursor process is aimed at producing thin films of superconducting oxides.

METAL-SPINNING. In the metal-precursor approach, American Superconductor starts with solid forms of the elements yttrium, barium, and copper, heats them to the liquid stage, then mixes them to form a liquid alloy that subsequently solidifies. One step in the process involves melt-spinning, during which a stream of the liquid alloy is directed onto a spinning vertical wheel. Heat is extracted during spinning, quenching the alloy into a solid form that spins off the wheel and is wound as ribbon onto a coil. The ribbon is then exposed to oxygen gas at a high temperature to form the superconducting oxide microcable.

Yurek maintains that the technique has advantages over the standard ceramic "shape-and-bake" methods that usually use powdered forms of YBCO. "Our process produces ribbon that has much better fabricability in the alloy state. It's also much denser and less brittle than is possible using ceramic processing techniques," he says.

In the polymeric-precursor process, American Superconductor makes a viscous liquid polymer containing metal citrate chelates formed from appropriate metal salts, citric acid, and ethylene glycol. The solutions are used to coat substrates and when heated, produce rigid metal-based resins. The resins are then fired to burn off the polymers, yielding the superconducting oxide. American Superconductor then uses spin coating, as in semiconductor photolithography, to produce continuous thin films on substrates made of strontium titanate, magnesium oxide, and yttrium-stabilized zirconia, as well as others.

Superconductivity may be as challenging now as laser technology 25 years ago

Neither process is mature, Yurek says. "We're going through active development programs with both processes to improve the properties of products—both mechanical and electrical properties."

Confidence also exudes from executives at startup Superconductor Technologies, Santa Barbara, Calif. The company's confidence may stem from its stellar lineup of backers and scientists. They include board members Robert Noyce, cofounder of Intel Corp., and Bob Schrieffer, a Nobel laureate in superconducting theory. The company has also named as president, CEO, and chairman Herbert Dwight Jr., who was a cofounder in 1961 of Spectra-Physics Inc. and its CEO until recently. Dwight likens the challenges of developing superconductivity as "similar to those faced by laser companies 25 years ago."

Superconductor Technologies already has the technology in place to develop the commercial niche products within several years, Dwight says. "People who get a toehold will be able to grow into a very significant enterprise," he predicts.

One company that thinks it can produce high-quality superconductive materials with its unique explosive process is Monolithic Superconductors. Its approach is to develop simple geometric shapes of superconductive materials with a range of applications. The process involves using the high-pressure state of a controlled explosion to consolidate superconductive powders by bonding them to a metal matrix. The company produced prototypes of copper and aluminum containing a variety of superconducting oxide ceramic channel geometries. "What we're looking at is the formation of continuous rings, linear or planar arrays and chan-

THE CHALLENGE: MAKING THE NEW SUPERCONDUCTORS BEHAVE

Researchers face a long and bumpy road developing materials that can be easily manufactured in a usable and consistent form as high-temperature superconductors.

All the new materials investigated so far have been brittle and environmentally sensitive ceramics. But they have many other properties that perplex researchers:

- They are anisotropic—their resistance to current flow depends on the current's planar direction. This characteristic is attributable to the material's grain boundary orientation.
- It is difficult to get large homogeneous quantities of materials in a single phase, so that the entire surface or bulk becomes superconducting.
- Most processes require a high-temperature annealing, which adds difficulty to manufacturing and affects the material's properties.
- Most of the materials are easily contaminated by water vapor, carbon dioxide, and other atmospheric agents.

In attacking these problems, researchers have been working exclusively with oxides of copper laced with other elements such as yttrium, barium, lanthanum, bismuth, or thallium. But scientists at Bell Laboratories have now detected superconductivity at 30 K in compounds without any copper, an example of new discoveries that confound workers in this field.

They are brittle and environmentally sensitive, and that's only the beginning

There has been slow but often surprising progress in discerning the superconducting capabilities of materials. Compounds discovered by IBM Corp. researchers J. Georg Bednarz and Karl Alex Müller exhibited critical temperatures of 35 K. Then, workers at the University of Houston, led by Paul C.W. Chu and Maw-Kuen Wu, discovered that a mixture of yttrium and barium in copper oxide (YBCO) would superconduct at 94 K.

With that breakthrough, superconductivity could for the first time be attained at simpler and cheaper-to-maintain liquid-nitrogen temperature (77 K). As a result, YBCO became the material of choice for many workers in the field today. More recently, compounds using bismuth and thallium have raised the critical temperatures to 110 K and 125 K.

The materials are being explored in bulk form, thin films, and single crystals, with varying results. But high critical temperature is not enough in itself to make a material suitable for practical use. Maintaining the superconducting state also depends on critical values of applied magnetic field and current density.

Many applications dictate high critical temperatures and current densities. And recently current-density levels have been raised significantly with processing refinements. Densities as high as 10^5 A/cm^2 in a polycrystalline thallium-based material at 77 K have been reported at Sandia Laboratories in Albuquerque N.M. And Bell Laboratories and NTT in Japan have achieved densities of several million amperes per square centimeter with epitaxial films of YBCO on strontium titanate substrates. *–S.W.*

neled structures that would have applications in shielding, and also in computers, communications, and telecommunications," says CEO Lawrence Murr.

Monolithic Superconductors is also working with YBCO, and Murr does not minimize the difficulty. "We've found that no commercial vendors have been able to make single-phase high-purity YBCO," he says. "And no one can make it in bulk quantities. One of the problems of working with this stuff is you have to begin with high-quality, high-purity, single-phase material. If you don't have that, there's no way you can make a reliable reproducible device."

With this in mind, the company is developing a potentially high-volume output process to produce the powder using a freeze-drying concept. The YBCO mixture is sprayed into a liquid nitrogen environment. Murr says this produces the desirable high-quality, single-phase, very pure material. "The powder that we make with our process is better than the best powder that commercial people make in a batch process and sell at enormous prices. When you do susceptibility measurements [on commercial powders], you find that the Meissner fraction, or portion of the material that is superconducting, is about 30%. That means that one-third of the powder you buy is superconducting and the rest is junk."

The concept behind the explosive fabrication technique, as Murr describes it, is to get this rather uncooperative material into a matrix that has the strength required to allow management of the material's engineering properties. The process avoids the high temperatures required of conventional ceramic-to-metal bonding methods, which can destroy YBCO's superconducting properties. For the explosive, Monolithic Superconductors uses various forms of ammonium nitrate, which is low in cost. Modest amounts can be used to fabricate large volumes, Murr says.

'FORGET WIRES.' Murr believes the technique will overcome a lot of difficulties experienced by other companies that are pursuing the manufacture of wires with superconductive materials. "We can make conformal geometries in a metal matrix without using any wires, and produce a lot of magnetic configurations without using enormous numbers of windings. We're saying, 'Forget wires. Let's do it another way.' "

So far, the technique has only yielded planar arrays that could be considered in the class of thick films. But it has potential applications in circuit-board fabrication, Murr says. "With our technique, we can't go to a device scale, but we've been able to make some hefty structures that might be the basis of a superconducting computer. For example, if you had to put a fair amount of input power into a computer, we could fabricate a thick-film array with a lot of superconducting channel capacity for the runs that bring in the power. Then you could stack arrays of ICs or VLSI structures on top of that."

CPS Superconductor Corp., a three-month old spinoff of Ceramics Process Systems Corp. of Cambridge, Mass., is another small startup that believes it can lick the materials problem. Peter R. LoConto, president and CEO, says the company is focusing on the manufacture of bulk material in the form of wires, based on processes developed by the parent firm. The company claims to have developed flexible wires and a means of producing them in continuous lengths on a pilot scale. Loconto declines to reveal the product's parameters, but says, "It's well in excess of anything that's been out there."

A major push is to develop a high-volume, consistent manufacturing process

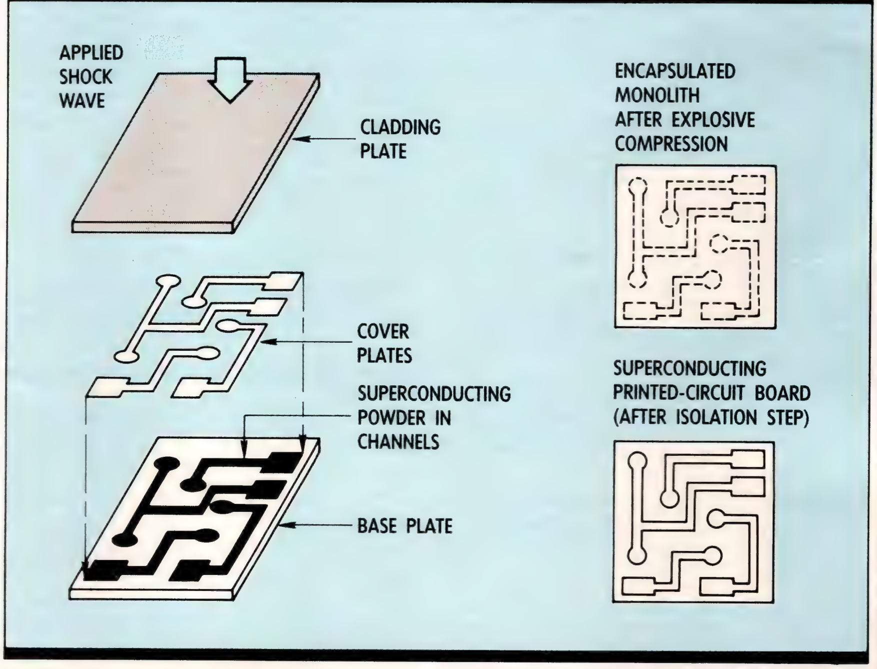
LoConto likens the situation to the development of fiber-optic technology. "Remember when we looked at glass as the medium for fiber optics and wondered how we were going to make it tractable? We solved that," he says. "Ceramic is also intractable. Making it tractable is the challenge." The company is the principal subcontractor under a Darpa-sponsored program for development of wire for a 50-horsepower superconducting motor.

One unique application being projected for superconductors is shielding against electric and magnetic fields in electronic systems. Monolithic Superconductors, with its explosive process, is pursuing planar sandwich arrays for magnetic shielding applications. And Electro-Kinetic Systems of Travis, Pa., a company that specializes in shielding materials, is delving into the application of superconductors to electric field shielding. The company supplies materials to makers of telecommunications devices and portable devices, says Jack Reilly, president and CEO.

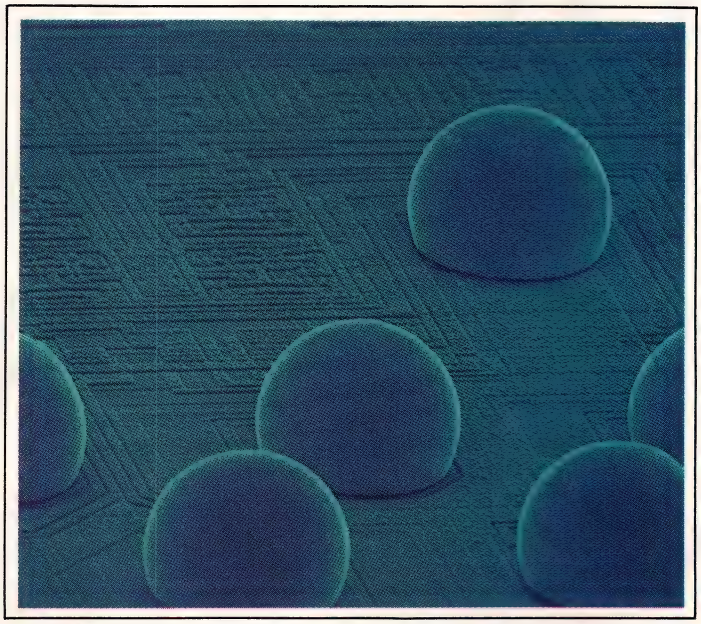
"Superconducting caught our eye about a year and a half ago, when we saw the temperatures going up, as applicable to electric-field shielding," he says. "Among the products we make are coatings and adhesives where we load conventional metal fillers into a plastic matrix, and treat them to get electrical continuity from particle to particle. Generally, the higher the electrical conductivity, the better the shield."

Reilly says that although it is far-fetched to think that superconductors will ever be able to work at room temperature, devices operate in cryogenically cooled systems now, such as large computers and most aircraft, carry liquid nitrogen aboard. Those kinds of environments could lend themselves to a shield using composites, he says. Electro-Kinetic Systems has only done some initial small-scale testing with YBCO because its work has no government support yet, he says. "We've proven that we can get better shielding than we can get with conventional composites," Reilly says, but the instability of the material remains a problem. ☐

MAKING SUPERCONDUCTIVE PC BOARDS



Monolithic Semiconductors is investigating how its explosive force technique could be used to form a superconducting printed circuit.



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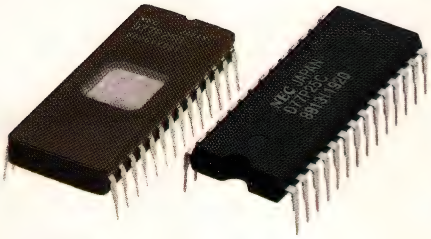

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TECHNOLOGY IN JAPAN: AN UPDATE

It's no secret that Japan is one of the world's great powers when it comes to electronics technology. From its outright domination of consumer electronics markets the world over to its more recently gained preeminence in semiconductor technology, the Japanese have excelled at all things electronic.

Now, in a time when Japan might be tempted to retrench and lick the wounds inflicted by its suddenly expensive currency—which has made Japanese goods far more expensive, particularly in its biggest export market, the U.S.—Japan is forging ahead with new technologies, new muscle, and new determination.

Japan's semiconductor industry is recovering well after a bad slump in 1985 and 1986, and capital investment is on the rise again; optical disk technology is catching on around the world as a data-storage format, and Japanese manufacturers are poised to exploit that rising interest; test and measurement equipment sales are finally picking up after two slow years—thanks, in part, to a resurgence in capital investment by semiconductor and computer makers. At home, Japanese personal computer sales continue to soar and the Integrated Services Digital Network, long considered to be a far-off dream, is about to become reality.

Only Japan's components industry is facing a difficult time, as its biggest customers—Japan's consumer electronics giants—have begun to search the Orient for cheaper places to build their equipment. As a result, components makers also have had to start off-shore plants, in Taiwan, Singapore, Malaysia, South Korea, and elsewhere, these firms have begun to set up shop alongside their customers, adding to the globalization of the world's electronics industries.

This report was prepared by the Nomura Research Institute in Kanagawa, Japan, under the direction of Shigeaki Kaneyori, who also wrote the update on Telecommunications. The Computer & Peripherals report was written by Yasuhiko Arai, the Optical Disk update by Shin Kusunoki, and the Semiconductor analysis by Juro Toda. Hisami Matarai produced the Components report, Shinya Uchida wrote the review of Pattern Recognition Technology, and Hiroshi Fukui wrote on Test & Measurement.

Cover photo courtesy of Oki Electric Industry Co.

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COMPUTERS & PERIPHERALS

NEW RIVALS EMERGE IN JAPAN'S PC WAR

The world of mainframe computers has been quiet in Japan in recent years, but the world of personal computers is still undergoing an explosive period of drastic change. The news in computers these days is coming from one place, and one place only: the booming PC market.

Japan's PC business has thus far been dominated by NEC Corp., which, like IBM Corp. in the U.S., has attained an almost unassailable position in the market. NEC's share of the 16- and 32-bit PC market exceeds 50%, and is even bigger when the market is pared down to include only stand-alone units. Such support has allowed NEC to construct a separate PC culture in Japan around its PC9801 family, a culture different from the one IBM Corp. has created in much of the rest of the world with its PC-DOS operating system.

Although numerous computer manufacturers have attempted various countermeasures to break NEC's grip, these have not only proven ineffective, but have even acted to increase NEC's leading share in some cases. Recently, however, two competitors have arrived on the scene to challenge the PC9801: AX and TRON.

AX is a Japanese-language version of IBM's PC/AT. A group of companies headed by Microsoft Corp. of the U.S. have established the AX Conference, which will determine standards issues ranging from hardware specifications to operating systems and application software. Already the group has lured 20 hardware manufacturers and 63 software makers into the project and that number could exceed 120 companies all told.

The AX mission is to stimulate the rise of the PC/AT, already the de facto international standard architecture worldwide, to become the standard in Japan too. But the other issues involved include eroding NEC's near monopoly. Though some experts think the idea of fresh development based on the PC/AT compatible architecture would be outmoded, AX aims to be far more than that. The system would be fully capable of supporting OS/2 system software, so the group believes the technology could support at least a five-year life cycle.

NEC CORP. FACES THE CHALLENGE OF AX AND TRON

The AX's impressive array of functions may be exemplified by its accommodation of Japanese-language processing. With the AT-compatibles that are now available in Japan, such as Toshiba Corp.'s J-3100 (the Japanese version of its T-3100), using Japanese-language processing requires the Japanese-language version of the MS-DOS operating system; if a user wants to be able to work in both Japanese and English, he needs both the standard MS-DOS and the Japanese version.

By contrast, AX is closer to the Apple Computer Inc. Macintosh environment, in which the processing language is stored in the form of a library. So the final AX operating system can operate independent of the end-user's language preference, because the language is effectively separated from the operating system.

Already five companies, attracted by the potential of adapting PC/AT-compatible factory-control software for the new system, have announced AX products: Sanyo Electric, Sharp Corp., Mitsui & Co. (through Alps Electric), Mitsubishi Electric Co., and Japan Acer. In addition, Canon Corp. has announced that its PC product—called NAVI—will be commercialized with AX specifications.

Garnering much attention lately, NAVI is capable of multitasking and comes equipped with telephone and facsimile functions, as well as a windowing capability not unlike that of Apple's Macintosh. The unit, which also features an innovative touch-panel for easier operation, will be released to the U.S. market in 1989, and Canon is hoping the NAVI will become the terminal of choice once Integrated Services Digital Networks are in place in the 1990s.

The other challenger to the domination of NEC's PC9801 is TRON, The Real-time Operating Nucleus, which was developed by Ken Sakamura, an assistant professor at Tokyo University. As a concept, TRON is a grand scheme of shared architectures combining personal computers, minicomputers, mainframes, communications systems, and other wide-ranging hardware implementations.

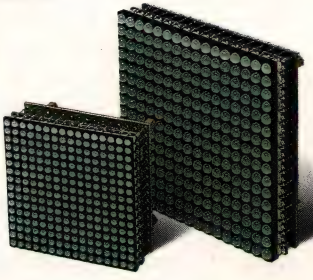
Business TRON, or BTRON, is the part of the idea that deals with PCs. BTRON is a PC designed to provide a uniform

Toshiba LED Module Achieves Delicate Display with 16-Gradient Control.

The forms and functions of information and its handling are diversifying with great speed. Toshiba, a world leader in the opto-electronics field, has developed a 16 × 16 LED dot matrix module that opens new possibilities in information display. By combining these modules, a display equivalent to that of a TV can be realized. By use of Toshiba's outstanding two-color LED together with its unique gate array for driving, 16-gradient control is achieved in this new product. Compact design makes the module lightweight and optimally thin. Unique heat radiation design greatly improves the dispersion of heat from the module, and connections are simple, ensuring freedom from maintenance. In applications ranging from simple messages to visual displays such as message boards, entertainment and projector use, Toshiba's LED module is a standout.

CHARACTERISTICS	**DETAIL**					
Type Name	TLMM501B2	TLGM501B2	TLSM501B2	TLMM502A1	TLGM502A1	TLSM502A1
Color Display*	Red, Green, Amber	Green	Red	Red, Green, Amber	Green	Red
Dot Size	∅5mm			∅3mm		
Dot Pitch	6mm			4mm		
Weight (Typ.)	170g	165g	165g	95g	85g	85g

*Amber color is made by a mixture of red and green.



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TOSHIBA CORPORATION: 1-1, Shibaura 1-chome, Minato-ku, Tokyo 105, Japan Tel: 03-457-3463

Circle 119 on reader service card

operating environment, regardless of manufacturer or model, by describing the display, operating modes, user interfaces, application interfaces, and operating system. The goal is to create a Japanese version of the Macintosh, complete with a variation of Apple's Hypercard concept.

BTRON has already been authorized as the official standard PC for Japanese classrooms, and Fujitsu, Hitachi, Mitsubishi, Matsushita, and Oki have all launched development programs based on the BTRON concept. Anticipating a huge market opportunity, these companies are trying to cash in now. According to the Japanese Ministry of Education, the market for school-based PCs will be in the several hundreds of thousands in the early 1990s. With present Japanese PC demand in the 1.2-million unit range, that's a sizable percentage. And students raised on BTRON machines are likely to continue to use it in their careers.

In support of BTRON, manufacturers are developing their own versions of a TRON microprocessor, a 32-bit chip that would be the heart of any TRON system. Hitachi is expected to be the first out of the box with a TRON microprocessor that will ship late this year. On its heals are Fujitsu, Mitsubishi, Toshiba, Matsushita, and Oki.

NEC isn't sitting while others chip away at its market leading status, however. By incorporating the added features of Microsoft Corp.'s OS/2 software ahead of the competition, NEC is hoping to get an edge in that segment of the market before its competitors even know it is there. The key to its strategy is the pending introduction of an OS/2 compatible machine based on Intel Corp.'s 80386 microprocessor.

Another part of NEC's strategy may be to turn its eye toward selling its PC/AT-compatible PCs to Japanese customers. These machines have been successful entries into the U.S. market for NEC, but the company has shied away from Japanese sales so as not to impact its 9801 sales. To get around that, some experts expect NEC to offer a hybrid machine that is compatible with both its own 9801 and IBM's PC/AT in the fall.

The Japanese Computer Market Looks For Continued Steady Growth

Type of System	1986	(millions) 1987	1988
Personal computers	$ 2,794	$ 3,104	$ 3,534
Technical work stations	1,160	1,867	2,758
Office computers	2,960	3,091	3,287
Minicomputers	1,072	1,108	1,182
Superminicomputers	494	574	663
Mainframe computers	11,107	12,775	14,846
Minisupercomputers	18	36	80
Supercomputers	227	315	373
Total	19,832	22,870	26,723

THE FALLING COST OF RIGID DRIVES ROCKS THE PC MARKET

But just as NEC is getting ready to protect itself from PC/AT compatibles and TRON, a third challenge is beginning to rise up: PC9801 clones. Seiko-Epson, for example, is selling a PC9801 clone that is vastly cheaper than NEC's unit in terms of price and performance. Like Compaq Corp. in the U.S., which challenged IBM first with a portable PC-compatible model, Seiko-Epson is challenging NEC with a lap-top 9801-clone that is holding firm in the market, even though NEC has followed with a lap-top version of its own. Although copyright problems are not resolved yet, other companies are expected to follow Epson into this market, and Kawasaki Steel is marketing a chip set that it says is compatible with both IBM's PC AT and NEC's PC9801.

Another factor rocking the Japanese PC market is the growing use of rigid, or hard, Winchester disk drives. The declining price of these drives, coupled with increasing demand for storage capacity, is behind this change. Prices for 5.25-in., 20-Mbyte hard disks stood at around $1,500 in early 1987, but they began falling at the end of the year so that consumers shopping in Tokyo's Akihabara district can now pick up the same disk for only $540. Denser 3.5-in, 40-Mbyte models are picking up steam, meanwhile, and manufacturers are claiming growth rates for these products in the 80% range. With Seagate Technology's Japanese affiliate planning to begin sales of these drives later this year, that rate should continue to climb. And 3.5-in. drives seem to be poised to take control of the market for built-in hard drives—those installed in a PC at the factory.

Laser printers, meanwhile, have not enjoyed the same runaway success. Although the Japanese market for laser printers is growing, few products have shown up equipped with page description language—PDL—functions. In fact, even when they are available, they often go unused. With desk-top publishing still in its infancy, there is very little software available to take advantage of the laser printer, and development of such software has been delayed by the inherent complexities of the Japanese language, which has 60 times more characters than English, including a large number of extremely complex ideographic characters, called Kanji.

Still, Adobe is developing a package called Postscript that is expected to be adopted by NEC, Fujitsu, Ricoh, and Matsushita Electric Industrial, suggesting that 1989 should bring the first laser printers equipped with Japanese language character generation. Canon and Toshiba, meanwhile, are expected to adopt PPCS, a Postscript-like product, developed by Phoenix Technologies. With software, these machines will cost in the neighborhood of $15,000.

Further development of desktop publishing systems in Japan awaits the wider availability of 32-bit PCs capable of processing the Japanese language at sufficient speeds, experts say. If that's so, laser printers won't really take off in Japan for several years.

Computer makers should come to look back on 1988 as a robust year. Overall consumption of computers and peripherals—including everything from PCs and small printers to mainframes and disk drives, will rise by 15%, reaching more than $58 billion. Steady growth is expected in virtually every sector, with some of the biggest growth coming from computers.

Total Japanesee computer consumption, including only non-captive production and using factory prices for domestically produced equipment and landed costs for imported products, will exceed $26 billion this year, according to market analysts (see chart, p.120).

The biggest growth will be in the fast-paced technical work station market, where sales will leap almost 48% to $2.76 million this year, up from $1.87 million in 1987 and $1.16 million in 1986. Also on a fast growth pace are superminicomputers. Although they still own only a very small portion of Japan's computer market, sales will more than double this year, from around $36 million in 1987, to around $80 million, making it a strong product area for the 1990s.

OKI HAS A YEN FOR STRATEGIC ALLIANCES

Masao Nogami, Senior Managing Director

Throughout OKI we emphasize the importance of developing strategic alliances with our customers," says Masao Nogami, senior managing director at OKI Semiconductors and Electronic Devices Group. "We regard a strategic alliance as a long-term business relationship which benefits both parties by enhancing our individual business strategies."

But strategic alliances are not automatic. They do not necessarily occur just because a customer represents large revenues to OKI. "On the contrary," Nogami says, "customers of relatively small size today may be the catalyst to point us to the next level of system technology. That is the key." Customers who team with OKI challenge it to press for greater technological advancement and greater synergy of existing technologies, he says. "We are committed to this idea because it demands more of us."

Within OKI there is a vast resource of products and technologies. The challenge the company seeks is to integrate these assets with new investments in mutually beneficial ways for both itself and its customers. "When OKI combines its CMOS technology, new gallium arsenide developments, an automated fab assembly, packaging expertise, design automation, and advanced board-level capabilities," Nogami promises, "a great range of solutions can be brought together to provide a full systems-level solution."

OKI's aim is to get customers to help innovation in a practical way. "If our emerging technology is field-proven by our early-adopting customers, then its usefulness is validated," Nogami explains. "We prefer to focus our research and development where the market is going and customers are the best source of information to define that direction."

With a range of capabilities, one-stop shopping is OKI's target. Application-specific integrated circuits, plus OKI's standard product line of chips and board-level products combine to give the company a formidable profile. Not only can OKI provide expertise in these areas, Nogami says in conclusion, but it can also help out with certain application expertise. "We can also add our applications knowledge in telecommunications and data processing to more fully utilize the broad capability of our company," he says.

OPTICAL DISKS CAPTURE JAPAN'S IMAGINATION

Optical disk technology has captured the imagination of Japanese suppliers in the last several years. Both audio and video formats have developed strong followings and rich markets in Japan's booming consumer electronics trade.

The compact disk, in particular, has found wide penetration in the audio market and growth is only now beginning to level off from the soaring rates of a hot new market to that of a more mature and saturated one. On the video front, a battle between formats continues, with no sign of a clear winner in sight.

The laser video disk format, developed jointly by Pioneer and Philips of the Netherlands, has been trying, without much luck, to challenge the dominant video disk standard, JVC's Very High Density (VHD) format. The two camps are locked in a battle not unlike the Beta-VHS struggle of the 1970s and early 1980s that left Sony Corp. alone in a losing battle against virtually everyone else. In the end numbers won out over quality, and even though many people acknowledged the superiority of the Beta format, VHS was the clear winner. In video disk technology, Sony is once again fighting the majority, thoug it is joined this time by Pioneer, and Yamaha in the battle against the dominant VHD camp, where JVC is backed by Matsushita Electric Industrial Co., Sharp Corp., Sany Electric Co., and several other leading manufacturers of consumer electronics products.

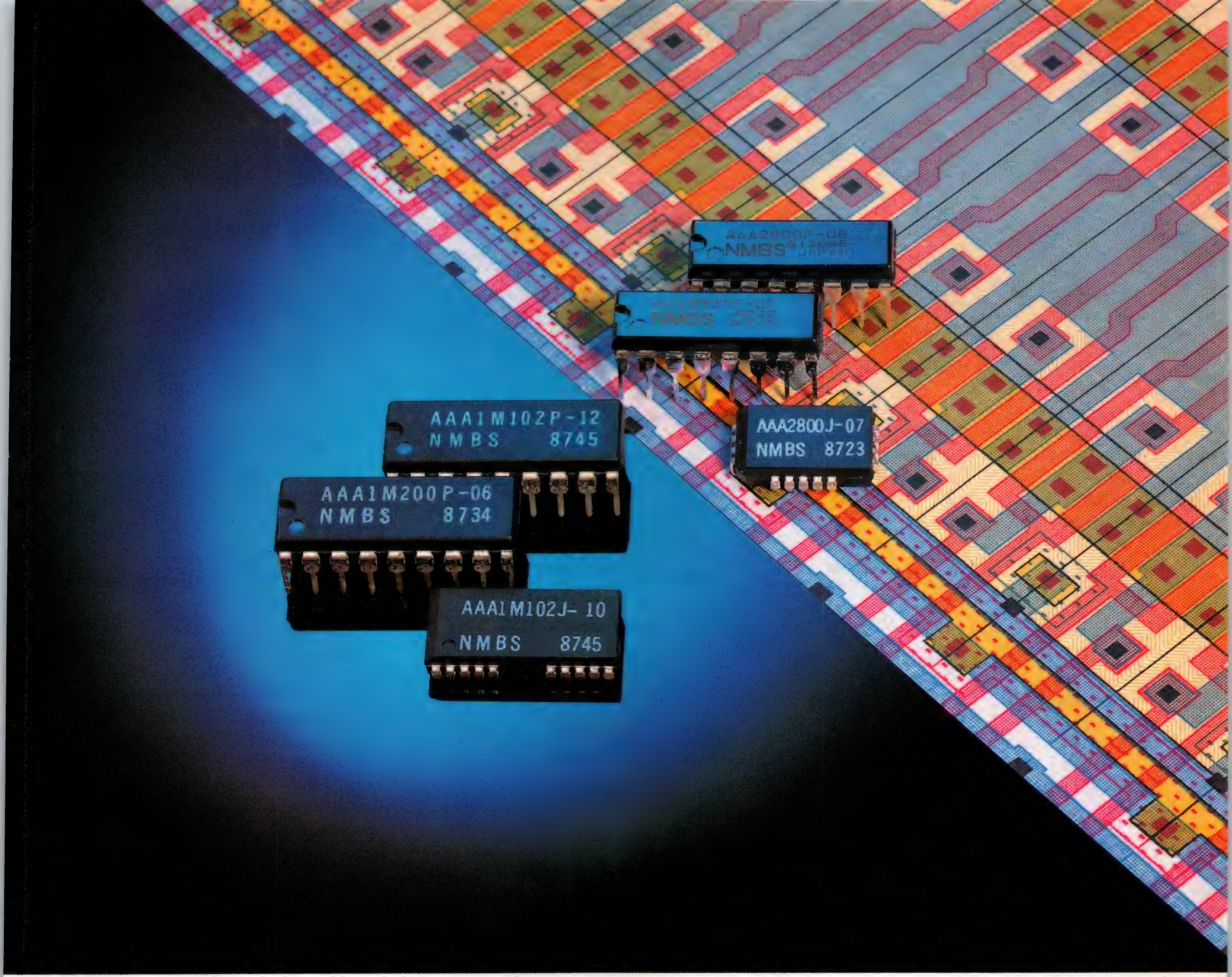
Things are beginning to change now, however, because of recent breakthroughs in digital technology. As the technology has improved, so too have the laser disk's chances to take the lead away from VHD. That's because the laser disk is compatible with digital audio, such as that on a CD, and VHD is not. So now Pioneer and its followers have begun to produce disk drives capable of playing back both audio CDs and video disks.

More recently, that has paved the way for players that could play three formats: CD audio, laser disk video, and the newest format on the block, CD-V, or video compact disks. The result? Laser-disk naysayers are eating their words as the technology solidifies its market position.

Laser disks, however, have not reached a saturation level anywhere near that of the VCR.

Planned Optical Disk Product Releases

Company	Disk size	Status
Sony Corp.	130 mm	Sample shipments underway; sales to begin in October.
Sharp Corp.	130 mm	Sample shipments underway.
Nippon Kogaku	300 mm	Sample shipments underway.
Olympus	130 mm	Sample shipments underway.
Matsushita Communications Industrial Co.	130 mm	Sample shipments underway.
Matsushita Electrical Industrial Co.	130 mm	Prototype announced; commercialization under study.
Maxtor Corp.	130 mm	Sales to begin in November.
	90 mm	Built by Seiko-Epson Corp.; Sales to begin in November.
Verbatim (subsidiary of Eastman Kodak Co.)	89 mm	Prototype announced.
LMSI	130 mm	Prototype announced.
Ricoh	130 mm	Sales begin in September.
NEC Corp.	N/A	Under development.
Fujitsu Ltd.	N/A	Under development.
Hitachi Ltd.	N/A	Under development.
Toshiba Corp.	N/A	Under development.



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OPTICAL DISKS GAIN SUPPORT FOR DATA STORAGE

1987 Japanese Production of Optical Disk Drives

Category	Sales (millions)	Unit Volume
Standard CD drives	$2,076.9	10,800,000
Reproduction-only video disk drives	446.2	429,630
Write-once read many (WORM) drives	176.9	11,500

Video buffs can rent video tapes for their VCRs for just 200 yen or so, roughly $1.50, but like in the U. S., rental shops don't carry laser disks—even though the video image is brighter and clearer. Those interested in the disks must purchase them at the steep rate of between $50 and $75 each. For now, laser and other video disk formats will have a tough time boosting their presence in the video field, experts say, unless they can come up with a better way to distribute their software.

All that aside, what's really exciting major Japanese equipment makers is the prospect of writable optical disks. Almost all of Japan's consumer electronics giants are joining the race to develop two types of writable disk technology—the write-once, read-many times, or WORM, drives, and the rewritable optical disks that act for the most part like optical Winchester disk drives. The difference, though, is great: optical disks have 10 times the capacity of their magnetic counterparts.

WORM products first appeared about five years ago, in the form of turnkey filing equipment for document storage. Toshiba Corp., Mastushita Electric Industrial Co., and Hitachi Ltd. all offered systems that combined electronic scanning equipment with the WORM drive. Targeted in the U.S. as a replacement for microfilm, these systems have not done so well in Japan, where microfilm penetration is not so great.

The first general-purpose 5.25-in. WORM drive for personal computer data storage hit the market in 1986. Produced by a U.S. manufacturer, Information Storage Inc., the unit was quickly followed to market by similar introductions from the likes of Hitachi, Matsushita, Ricoh, Mitsubishi Electric, and Pioneer. Each of these drives used its own distinct format. Realizing that widespread market penetration would depend on their ability to work together to define a common standard, the companies worked together through the ISO—the International Standards Organization—to define a uniform standard for 130-mm WORM drives.

Although the move to standardize marked one of the first times such a diversified group of companies ever tried to come together before a real market had become established, the attempt only served to drive home the great difficulty involved with bringing so many factions together. The ISO did prepare draft standards last October, but these were the product of compromise, and do not represent a single uniform format. The draft had to be broad enough to accommodate many many different types of products and assurance of data compatibility across all of those products is all but impossible.

So today, a number of manufacturers are hard at work on applications systems incorporating various unique WORM formats, targeting everything from data storage for computer-aided design systems to backup for digital copiers. But WORM technology has limited application for most computer users because most software takes for granted the presence of fully erasable disk storage. Hence the heavy interest in rewritable optical disk technology.

The first rewritable optical disks came out of a joint development effort between Kokusai Denshin Denwa (KDD) and Sony Corp. Both Sharp Corp. and Sony, among others, soon followed with full-fledged marketing efforts for 130-mm drives that could be used as disk storage in large computer systems. Now more than a dozen Japanese companies have entered this crowded field and are planning 1988 product introductions.

Although optical disk drives have been criticized for slow access speeds, Maxtor and Matsushita have recently begun to show prototypes that aim to solve that problem. Sources say these new disk drives will feature access times less than 30 microseconds by separating the optical head from the drive unit. The reduced weight helps speed the scanning process. Winchester disk drives are still roughly 50% faster than even these optical drives, but the improvement is expected to give the optical disks more competitive muscle when speed is only of marginal importance.

Now that numerous companies are ready or nearly ready to begin offering samples of their new rewritable disk drives, emphasis is expected to shift toward finding and developing applications for the technology. And once the application groundwork is complete, the stage will be set for rewritable optical disk technology to take off in the 1990s.

SEMICONDUCTORS

JAPAN'S CHIP MAKERS: INVESTING ONCE AGAIN

The top six Japanese chip makers cranked out total production worth more than $15.3 billion in the 1987 fiscal year, passing—for the first time ever—the 2-trillion yen mark. With demand picking up early in '87, the stage was set for a full-fledged recovery in 1988.

A booming market for office automation equipment both in Japan and abroad is fueling the present surge, but other factors include a world-wide rush to upgrade office equipment after two years of minimal growth and the rapid escalation in the use of automotive electronics. With high hopes for continued growth through the end of this year, Japan's mighty chip makers are calling for a double-digit production boost over last year.

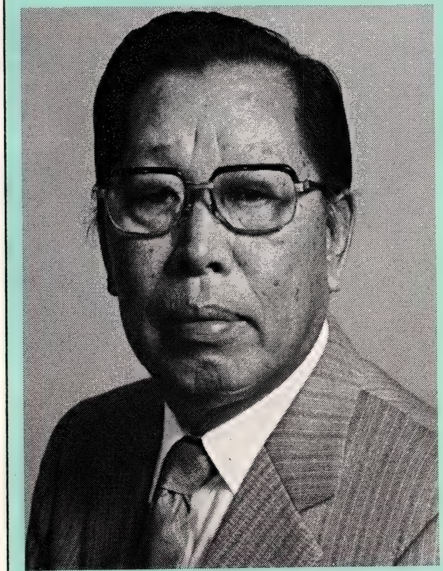
Such strong growth is encouraging chip makers to invest heavily in capital equipment. For the first time since the downturn of 1985, capital investment by Japan's leading chip makers is rising. The resulting picture is one of vigorous investment designed to respond to the shortages that have hit the markets for such popular devices as dynamic random access memories.

Nevertheless, the past bout with surplus investment, which many people blame for the bad times of '85 and '86, has made manufacturers wary about making the same mistake again. The current round of investment, therefore, is centered on reinforcing production of 1-Mbit DRAMs and other high-volume chips for which the risk of shortage is particularly serious.

NEC Corp. is boosting capital

NMBS CONCENTRATES ON CMOS MEMORIES

NMB Semiconductor is the only Japanese manufacturer dedicated exclusively to developing and marketing sophisticated CMOS memories and has rapidly emerged as the world's uncontested leader in high-speed memory devices, with access times of 60-, 70-, and 80-ns.


Takumi Tamura, President

NMBS is currently developing or marketing dynamic random access memories with densities ranging from 256-Kbits to 1- and 4-Mbits, static RAMs of 64-Kbit and 256-Kbit densities, video DRAMs, and other memories.

NMBS's Tateyama plant is the most advanced very-large-scale integration CMOS production facility in Japan. The second phase of the plant's Module II began operations in March 1988 as part of NMBS's strategy to increase its production capacity to 1 million 1-Mbit DRAMs per month by the end of 1988. Module I of the plant boasts Class 1 clean rooms, which make extensive use of robotics, and is capable of wafer fabrication of circuits with 1-micron geometries. Module II has even higher automation levels and sub-micron processing capability.

NMBS's Microfabrication facilities feature a 5:1 projection and exposure system; a high-performance, fully-automatic photolithography system; single-wafer plasma-etching equipment; a complete range of chemical vapor deposition systems; and high-performance test and measurement equipment. The company's advanced design, processing, and testing technologies are all aimed at ensuring the highest possible reliability and quality.

NMBS is working to increase production capacity to meet the rapidly expanding needs of the computer industry, particularly manufacturers of 32-bit personal computers. These companies need high-speed memory chips to take full advantage of today's faster, more powerful microprocessors. The addition of Module II at the Tateyama plant, combined with an overall doubling of NMBS's staff, are both aimed at meeting this growing demand.

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Oki is ready to help you speed product development, improve your production efficiency and shave costs with integrated system technologies and constant technical support. Oki is more than a one-stop source of the highest-quality electronic devices and state-of-the-art ASIC design and production. We provide total project assistance, from design and manufacturing of system components and modules to technology assistance, available at any development stage, through design centers in the U.S., Europe, and Asia.

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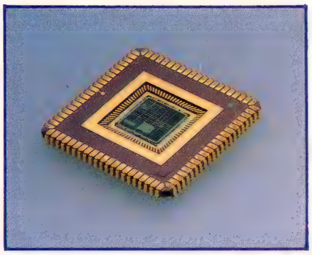

Oki leadership in advanced IC manufacturing is based on a commitment to the future — through the development of 4M DRAMs, a submicron CMOS process, and now, design and production of high-density channelless gate-arrays.

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investment in its chip business 25%, Hitachi Ltd. is increasing investment 45%, and Matsushita Electric Industrial Corp. more than doubled its capital investments in the chip business this year over 1987 (see chart, p. 128). What is the effect of all this investment on technology? It's been a stimulant, sources say, for such long-range leading-edge products as 16-Mbit DRAMs and sub-micron manufacturing processes.

In the memory business, NTT's announcement early in the year that it had developed a 16-Mbit DRAM started things off on a runaway pace. The disclosure was followed quickly by Hitachi, Matsushita Electric Industrial, and Toshiba, which all announced that they were doing their own development work on 16-Mbit DRAMs.

Matsushita's effort is the most ambitious: the company is using a trenched-capacitor structure and half-micron line-widths, the smallest of the competitors. Toshiba is also using a trenched capacitor design, but is incorporating it in a less ambitious 0.7-micron process. The result will be a chip twice the size of Matsushita's. Hitachi, meanwhile, is taking a two-track approach, studying designs based on both trenched and stacked capacitors. Hitachi isn't saying when it will decide between the two.

In static RAMs, the emphasis is in boosting the access times of 1-Mbit chips. The fastest parts to hit the street in Japan in the past year have been a 14-ns part from Mitsubishi Electric; a new chip from Hitachi, just a shade slower at 15-ns; and Fujitsu's 18-ns SRAM.

But perhaps the most stirring news in Japan is surrounding developments in 32-bit microprocessor technology. Causing the stir is the Japanese-developed operating system called TRON—The Real-time Operating Nucleus, for which specifications are now available. Hitachi, Fujitsu, and Mitsubishi Electric are all developing TRON microprocessors through a mutual technology exchange agreement. With an operating frequency of 20 MHz, the processors will be able to run up to 7 million instructions per second, thanks to bilayer aluminum wiring and 1-micron geometries.

WHO WILL BE FIRST OUT WITH 16-MBIT DRAMS?

Elsewhere in the logic world, NTT says it has used large-scale integration techniques to develop a prototype chip capable of handling speaker-independent voice recognition tasks. The 12-mm by 12-mm CMOS chip supports functions that will facilitate use by financial institutions, which are interested in the technology for telephone banking services that would employ secret account codes.

Still another logic development comes from Sharp Corp. and Mitsubishi Electric Co., which have developed concurrent processors in a data drive format. These 1.2-micron CMOS parts use double-layer aluminum metalization and are characterized by function division among the parts' major elements.

Gallium arsenide technology, meanwhile, is just beginning to pick up steam. Toshiba has begun shipping samples of a microwave communications integrated circuit that boasts an output of 12 W—the greatest in the world. The new chip operates in the 8.5 GHz to 14.5 GHz range.

For its part, NEC is developing a GaAs and aluminum-GaAs heterojunction bipolar transistor—HBT—that just might enable the realization of a completely monolithic transmitter/receiver IC for use in microwave and millimeter wave communications. These would be particularly useful in military radar systems, or in satellite reception and transmission. NEC

Japan's Leading Chip Makers

As production goes up . . .

Company	Sales (billions) 1986	1987	1988*
NEC Corp.	$3.54	$3.92	$4.46
Toshiba Corp.	3.15	3.62	4.00
Hitachi Ltd.	2.96	3.15	3.62
Fujitsu Ltd.	1.55	1.90	2.31
Mitsubishi Electric Corp.	1.35	1.69	2.00
Matsushita Electric Industrial Corp.	1.55	1.65	1.85

*estimate

. . . So too does capital investment

Company	Investment (millions) 1986	1987	1988*
NEC Corp.	$308	$308	$385
Toshiba Corp.	523	538	615
Hitachi Ltd.	231	308	446
Fujitsu Ltd.	168	305	362
Mitsubishi Electric Corp.	138	123	192
Matsushita Electric Industrial Corp.	192	169	400

*estimate

Coming in OCTOBER in ELECTRONICS

SPECIAL REPORT: **Technology Outlook**
Here's our annual outlook at what's going to happen to technologies over the next year in major market segments. Our readers get an update and outlook on everything from semiconductors to software, data communications to factory automation.

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REAL TIME: DSP Makes The Move. The software hurdles in digital signal processing and whats being done to overcome them. Industry managers will find out in October.

UPDATE: **The First 100,000- Gate Semicustom Arrays.** A look at what's happening with these giant arrays since they were first reported in *Electronics* a year ago.

A LETTER FROM: **Washington D.C.** Presidential elections... government spending... Sematech and more. Our man in Washington tells all.

MANAGEMENT EDGE: **Bonus Time.** Now that the black ink is back for many electronic suppliers, how are employees being rewarded, and what has changed since the last boom times.

EXECUTIVE BRIEFING: **Quantum-Effect Devices.** Will the quantum-coupled device be the successor to the transistor? Many think so. *Electronics* readers will find out which companies are pushing developments and how quantum-effect devices could impact the future.

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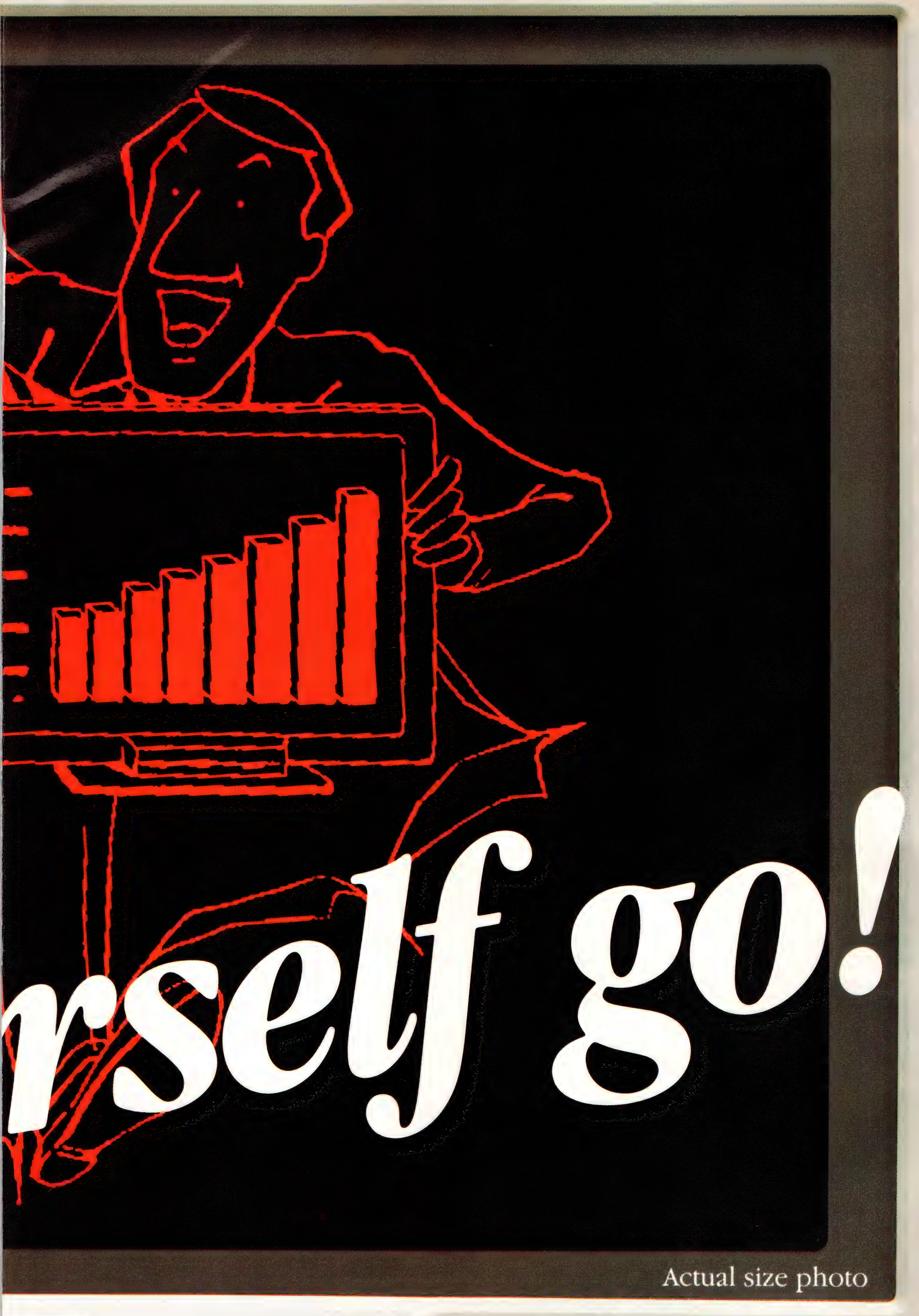
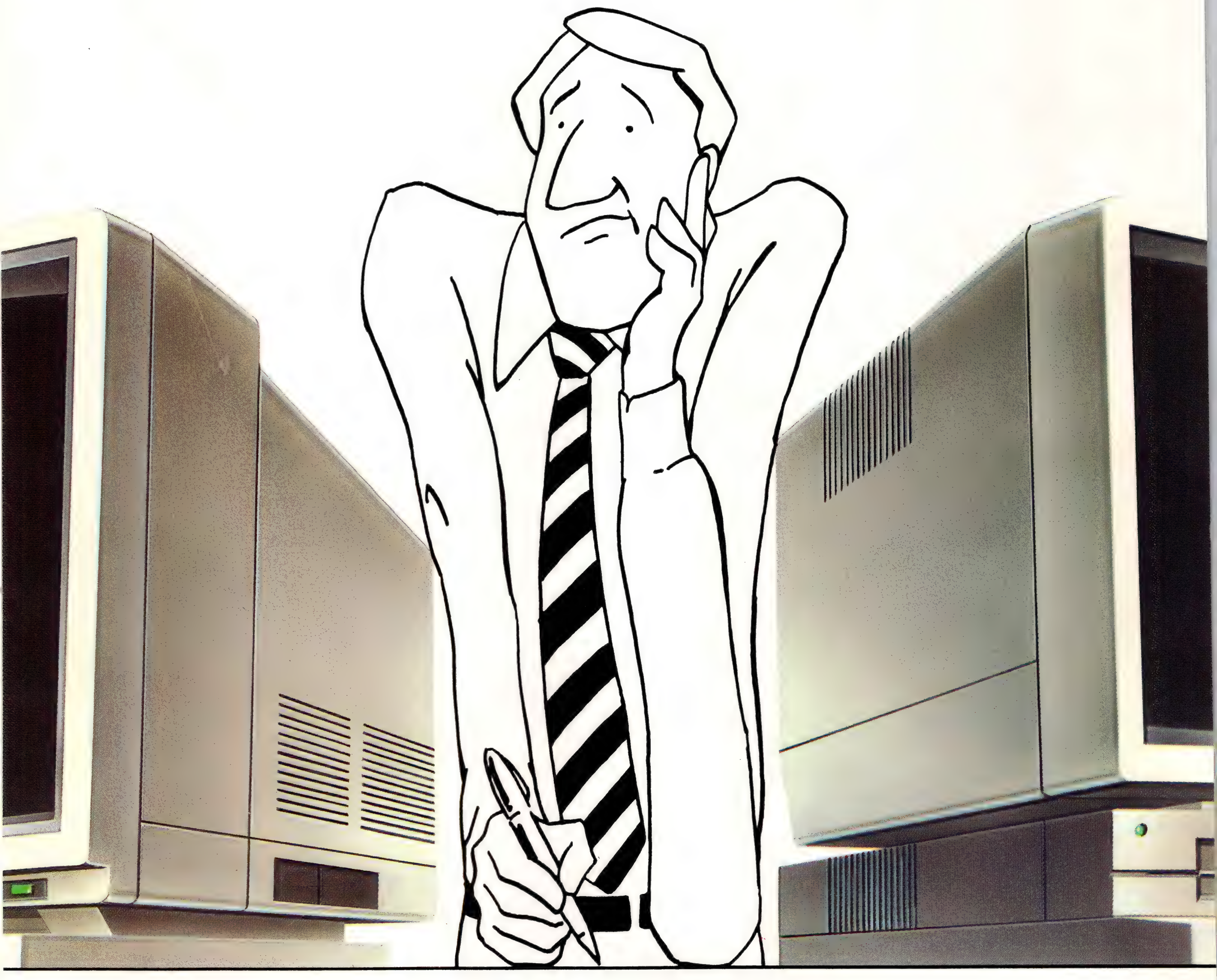


Actual size photo

Let you

A few words to anyone who's been held down by the size and weight of CRT displays:



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- **Illegal address detector**

This peripheral device was developed to reduce parts count in small systems based on Motorola's 8 bit micro processors. A system can be constructed from as few as 4 or 5 chips (MPU, EPROM, EXIO, and reset driver, plus an ADR latch for HC11 systems.) I/O can be expanded with 3, 8-bit latched outputs and one 8 -bit buffered input. Further expansion of I/O ports can be easily achieved by using two, three, or more MS68EXIO's per system.

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- **Input level ECL compatible.**
- **4 milliamps each channel**
- **FASTBUS segment driver**
- **Hybrid chip**

This hybrid circuit was developed as a line driver for high speed ECL systems based on the IEEE FASTBUS standard. It may be used in any application requiring ECL inputs and differential current driver outputs for long twisted-pair lines. Line receivers can be normal ECL receivers with terminators. Output current swing is 0 to 4 ma per channel, with 8 channels per circuit. Circuits are individually laser-trimmed for very low "off" current.

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claims that a 15-GHz transmitter with a hybrid composition based on HBT technology could improve integration, and hence reliability and cost, without a significant loss in signal clarity. NEC says phase noise would be curtailed to the same 65-dB level attained using conventional GaAs field-effect transistor technology.

NEC is also developing GaAs optoelectronic ICs—chips that integrate long-wavelength semiconductor lasers, or optical detectors, and solid state electronic circuitry. So far, these have performed successfully in optical transmission tests over distances up to 53.5 kilometers before the signal needs to be repeated. The target application is high-performance networks.

Further out on the cutting edge are chips built in superconducting technologies. Fujitsu has developed a 4-bit microprocessor, built from superconducting niobic materials, that integrates roughly 5,000 Josephson Junction devices on a single chip. NEC, meanwhile, has used the same superconducting materials to build a 1-K DRAM with about 1 million Josephson Junctions on board. Line widths are still on the order of 2- to 3 microns, but the technology shrink to 1 micron has already begun. The companies are expected to announce a 16-bit microprocessor and a 16-K DRAM in the next year or two.

Also far out on the horizon are three-dimensional chips—ICs that include several layers of elemental arrays stacked in a 3-D format. Such companies as Mitsubishi Electric, Sharp, and Matsushita Electric Industrial are developing prototype products using this technique designed for image processing applications.

Research and development of 3D ICs dates back to activities that began in 1981 at the Electrotechnical Laboratory at Densoken, where several firms collaborated on the effort. Several outstanding technical difficulties remain, particularly those associated with the formation of the interlayer isolation film and with monocrystalline growth on that film. But companies are beginning to talk about developing parts with practical applications by 1991 or 1992. The technology could start turning up in systems by the mid- to late-1990s.

Mitsubishi Electric, for example, has already succeeded in producing a prototype image processing chip integrating 11,000 circuit elements on a tri-layer structure. The upper layer contains an image sensor measuring 5 pixels by 5 pixels, the middle layer contains an analog-to-digital converter that converts the analog sensor data into digital form, and the bottom layer contains the logic to do the arithmetic functions high-speed signal processing demands. By combining so many functions in one chip, processing speeds are about 5,000 times greater than the two-dimensional solutions that address the same problem.

Japan's Big Appetite for Chips: Demand is Up 20% Over 1986

	(millions) 1986	1987	1988
Discrete, total	$ 3,124	$ 3,101	$ 3,319
Diodes, total	1,041	1,017	1,052
Microwave (above 1 GHZ), all types	31	29	29
Rectifiers and rectifier assemblies	514	515	542
Small-signal (less than 100 mA, including arrays)	274	251	252
Varactor (tuning)	112	114	120
Zener and reference	110	108	109
Protection devices	95	95	96
Thyristors (SCRs, Triacs, etc.)	201	196	207
Transistors, total	1,787	1,793	1,964
Bipolar, total	1,471	1,487	1,592
Power (more than 1 W dissipation)	667	695	748
Small-signal (including duals and arrays)	804	792	844
Field effect, total	194	197	202
Power (more than 1-W dissipation)	76	87	91
Small signal	118	110	111
Gallium arsenide	7	8	11
RF and microwave power (bipolar and FET, silicon)	115	101	159
ICs, total	12,629	13,323	15,586
Linear, total	3,466	3,508	3,931
Communications (including telecom codecs, etc.)	235	234	302
Consumer	1,975	1,984	2,166
Interface (drivers, buffers, etc.)	717	741	830
Op amps (monolithic only)	358	347	400
Voltage references	181	202	233
Digital, total	9,163	9,815	11,655
Custom and semicustom, total	1,579	1,895	2,217
Custom	623	647	701
Gate arrays	876	1,152	1,356
Programmable logic	80	96	160
Memories, total	2,525	2,749	3,247
Random access, total	1,691	1,821	2,145
Dynamic RAM	1,163	1,238	1,451
Statoc RAM	528	583	694
Read-only memory	834	928	1,102
Microprocessors and microcomputers	1,679	1,837	2,156
Special purpose	1,280	1,270	1,680
Standard logic families, total	2,100	2,064	2,355
BiCMOS	147	173	207
Bipolar	1,724	1,620	1,805
CMOS	229	271	343
Total	15,753	16,424	18,905

COMPONENTS

FOREIGN RIVALS PRESS COMPONENT MAKERS

Japan's $20 billion component industry, though not enjoying boom times, continues to enjoy steady growth of about 5% a year. This increase, however, depends on the high growth rates registered for production in certain market segments, such as printed circuit substrates and switching power supplies. In most other segments, production has leveled off. The extensive migration to foreign shores of consumer electronics production has also had its effect, causing severe fluctuations in some component markets.

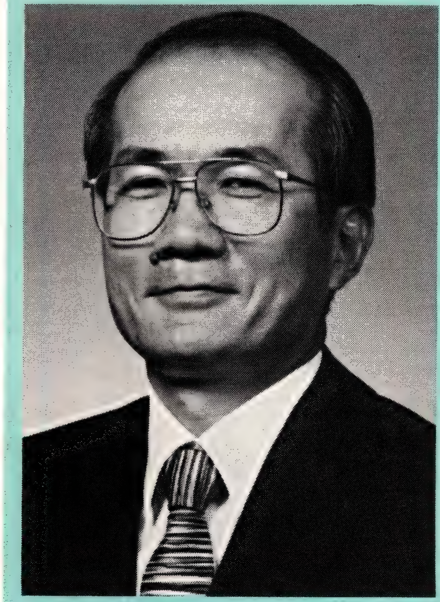
Japan produces about 35% of the electronic components used worldwide, according to the Electronic Industries Association of Japan. And when off-shore production by Japanese firms is added in, that figure approaches 40%.

Most of that is due to Japan's strength as producers of consumer electronics. In the market segments serving the consumer equipment industry, such as coils, resistors, small motors, magnetic heads, and ceramic condensors, the Japanese share of the world market often exceeds 50%. In those segments serving the industrial market as well, such as connectors and printed circuit substrates, the Japanese share is somewhat less than 35%. Japan has only about 5% of the U.S. market for components, for example.

SOME FIRMS GET FORCED OFF SHORE TO COMPETE

Japanese exports of basic components (not including those already assembled into other equipment) came to about 20% of total production, or around $4 billion in 1987. Exports in the form of kits sold by equipment makers in the same year accounted for an additional $1.2 billion.

FUJITSU: DIVERSIFYING FOR STRENGTH


Toshio Hiraguri, Director

Fujitsu Ltd. produced its first computer—a relay model—in 1953, long before semiconductors became the primary components of computers, says Toshio Hiraguri. Since then, he adds, the information industry has witnessed one technical innovation after another, and markets have grown enormously.

Fujitsu has continued to increase and improve its product lines and today it supplies a full range of products and systems—from the FACOM VP series of supercomputers and FACOM M series of general-purpose computers to office automation equipment, work stations, personal computers, and semiconductors.

Hiraguri says Fujitsu has traditionally followed a product and business development strategy aimed at integrating its multiple product lines. Fujitsu has always been an industry leader in the development of advanced semiconductor technology, for example, and the use of this technology, company officials say, has given its products superior quality, performance, and cost-effectiveness.

But semiconductor technology alone is not enough, Hiraguri explains. Fujitsu is also interested in integrating information and communications processing. Fujitsu started business as a telecommunications equipment manufacturer in 1935, and in its long experience since has produced sophisticated technologies and a wide range of products in the telecommunications field. Now, capitalizing on expertise in both computers and communications,

Japanese Production of Major Component Technologies

Technology	1985	1986	1987	Adjusted Annual Growth Rate
	($ billions)			
Resistors	2.08	1.94	1.93	−4.1%
Condensors	3.37	3.36	3.41	0.7%
Coils and Transformers	2.64	2.47	2.44	−4.3%
Switches	1.23	1.21	1.17	−2.5%
Connectors	1.39	1.46	1.57	5.8%
Small Motors	2.45	3.23	3.10	13.4%
Magnetic heads	1.40	1.48	1.47	2.3%
Printed Circuit Substrates	2.21	2.25	3.14	18.4%
Switching Power Supplies	1.15	1.31	1.58	16.9%
TOTAL	17.92	18.71	19.81	5.2%

These kit exports stem from the need to supply the overseas operations of Japanese makers of TVs and video cassette recorders. About 40% of those kits were exported to other Asian countries, 20% went to the U.S., and 15% went to Europe. The remaining kits were shipped to other locations around the world.

Imports, meanwhile, accounted for only about 5% of Japanese demand for components in 1987. Most of that came from other Asian countries—43%—and the U.S.—36%. In general, Asian imports were incorporated into consumer electronics goods, such as stereos and VCRs, and U.S. imports were destined for use in industrial equipment.

The soaring value of the Japanese yen has led to a sharp reduction of production levels of consumer electronics equipment in Japan. Production slipped 13% in 1987, to $28 billion, compared to 1986 levels, and 1986 represented an equal $40 billion decline from the peak in 1985.

But despite the shift of consumer equipment production to other Asian locales, component production in Japan has held steady. A corresponding increase in industrial demand has helped to soften the blow to the consumer market. And Japan's reputation and experience with low-cost components for consumer equipment has kept it competitive in supplying those customers that have shifted production to other shores. Finally, Japanese component suppliers have so far succeeded in keeping the bulk of their operations in Japan, holding back from making the major investments necessary to set up shop elsewhere.

Most overseas production facilities belonging to Japanese component makers are located in newly industrialized Asian countries, such as Singapore, where there are growing markets for parts destined for consumer electronics equipment. Japanese component makers meet that demand with custom- and high-

---

Fujitsu is developing products and systems that integrate the two technologies.

The idea is to become a total system supplier, offering everything a customer could ask for, according to Hiraguri. With a range of products that includes computers, work stations, networks, and system and applications software, the strategy is working, Hiraguri explains. The company places high priority on its systems engineers, who provide customers with carefully planned support right from the very beginning of the system construction stage. But Fujitsu support does not end there. It continues through the successful installation of a completed system and the ongoing support today's customers need.

Fujitsu has also put a lot of effort into adapting English-language computers to the Japanese environment. Today, computer processing with the Japanese language is a matter of course, largely because Fujitsu did prioneering work in systemizing Japanese language processing for general-purpose computers years ago. Without that innovative early work, Japan's computer industry might not be as vibrant as it is today.

The company's knack for developing the right product for the Japanese market at the right time, and its determination to develop superior products and systems has strengthened its position in Japan as the number one maker of computers—a position it has held for eight years running. Hiraguri hopes to apply the same creativity and commitment as the company enters what they call "the highly information-oriented society of the 1990s."

These officials predict that the coming decade will be one of continued technical innovation in the semiconductor industry, as chips become more and more integrated and sophisticated. Smaller line-widths and new processing technologies, will increase chip integration.

New uses for computers, in offices, factories, and homes, coupled with the spreading of advanced computer networks such as the Integrated Services Digital Network schemes now being implemented in future telephone systems, will help Fujitsu further its 53-year history of merging leading-edge technology with the growing needs of the market.

grade components sourced from Japan and high-volume, low-cost parts sourced from their third-world factories. Also, those parts, such as coils and motors, which are more labor intensive, are generally produced in the newly industrialized Asian countries.

The strong yen has had a major impact on Japanese component makers. In the resistor market, for example, companies such as Alps Electric and Hokuriku Electric Industries are moving more and more production off shore to South Korea, Taiwan, Singapore, and Malaysia.

Also moving off shore have been makers of aluminum electrolytic condensors, such as Japan Chemicon and Nichicon, which have moved work to South Korea, Taiwan, Singapore and Malaysia. Production in these countries, once limited to only the most basic of components, is now broadening to include even the most sophisticated electronic components.

Makers of Tantalum condensors, however, are staying put in Japan. That's because the end-products that use these components—consumer equipment such as camcorders and headphone stereos—are still produced almost exclusively in Japan. Without an off-shore market to penetrate, production for these parts has remained on Japanese turf.

Ceramic condensors, though, have not moved off-shore, and TDK, Murata, and Taiyo Yuden have all shifted production overseas. Much of this production has gone to the U.S., for use in automobiles assembled there by Japanese companies.

Likewise, labor intensive technologies, such as coils, switches, and transformers, have moved off-shore. But these were among the first components to be supplied to the Japanese from other countries, and foreign production of them is not new.

CONNECTORS ARE STILL A TOUGH MARKET FOR JAPAN

The connector business, long dominated by the U.S., continues to be a tough one for Japan. U.S. makers have boosted production in Taiwan and Singapore to meet the surging demand of makers of TVs, personal computers, and other equipment now being built there. But Japanese manufacturers, such as SMK, are beginning to try to meet the U.S. challenge by locating production in those countries too.

As for those companies producing switching power supplies, they've got their hands full just trying to meet demand in their home market of Japan. No extensive off-shore production shift is anticipated in the short-term, although some Japanese companies have begun limited production of the supplies in Taiwan and Singapore to meet the demand of their own PC-building operations.

In Europe, where some Japanese firms have begun making electronic photocopiers, local-content laws may force one or more companies to launch production of switching power supplies on the European continent within the next year or two. If that doesn't happen, the copier makers could find themselves paying import duties on equipment built in Europe, because the level of domestic content may not be enough to satisfy strict local laws.

All that aside, Japanese component makers are very aware they will have to fight to maintain their leading market positions. Rigorous cost cutting measures are now the rule, as is the shift to off-shore production. Indeed, total off-shore production by Japanese companies was up 38% from the 1986 level of $2.6 billion to $3.6 billion in 1987.

As long as the yen remains strong, Japanese component makers will have to continue down that off-shore path. The expensive yen will force Japanese manufacturers off-shore and if the component makers don't follow suit, they'll lose the business. But sentiments are now beginning to grow in Japan and elsewhere that the currencies of such countries as Taiwan, South Korea, and Singapore are undervalued relative to the U.S. dollar, and should be raised. If that happens, a further shift to other locales, perhaps including China, could be just around the corner.

PATTERN RECOGNITION TECHNOLOGY

IMAGE PROCESSING ATTRACTS INTEREST

Pattern recognition—the method by which a computer-based system analyzes either images, speech, or sound—can be broken down into two sub-categories: image processing and speech recognition.

Image processing is by far the more extensively used of the two, and over 100 companies now produce such systems in Japan. By contrast, speech recognition systems are used in only a few applications and work in this area is almost entirely under the purview of the major systems houses. The only major application of speech systems to date has been by NTT, which uses the technology in AANSER—its Automatic Answer Network System for Electronic Request—a service provided to financial institutions. Sharp Corp., meanwhile, has aroused attention with the recent introduction of a speech-to-text word processor.

Image processing systems, used primarily for inspection purposes in assembly line operations or other in-plant work, are primarily produced by either small venture firms or are imported from producers in the U.S. and elsewhere.

By far the biggest application for pattern recognition technology is automated inspection systems. The technology is useful there in identifying damage, defects, dirt or other foreign substances, or position errors. These systems are installed both as stand-alone units and as subsystems integrated into a larger system. Many of the systems now available commercially were developed originally for in-house use.

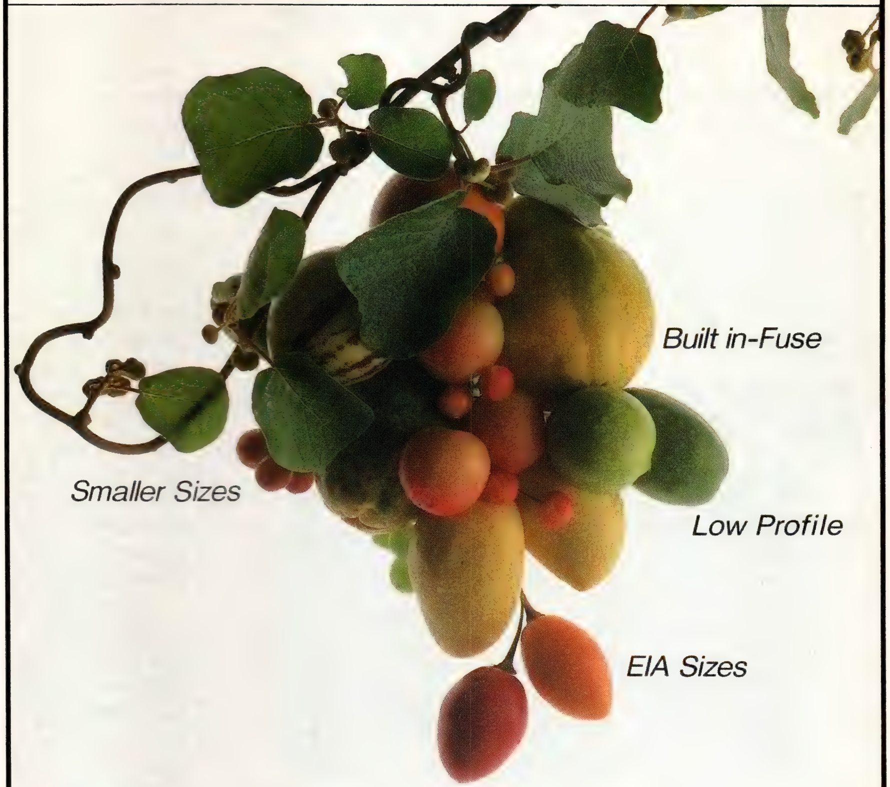
Venture firms will go so far as to tailor a custom system to a customer's needs, developing control software as well as the necessary hardware. Fujitsu Electric also offers such services, as do a few of Japan's other major manufacturers. Systems developed with this approach include one for inspecting the characters carved on lozenges developed by Kanebo; mask pattern inspection systems developed by and for semiconductor firms; Matsushita Electric Industrial Co.'s mounting systems for keyboard chips and components; and a label inspection system used by Kirin Brewery.

Image inspection systems are also used in sorting applications for agricultural and fishery products as well as for manufactured goods. In manufacturing, there is generally no distinction between inspection and sorting processes, and the same hardware is used for both applications. Fujitsu is the leader in this field.

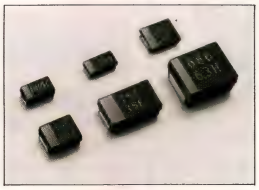
In practice, these systems are used either as a method of helping humans to see what the naked eye cannot distinguish or as a means of giving sight to industrial robots. Robots can be used to determine and adjust component position and attitude, matching of components with insertion holes, and controlling the distance between components mounted on a printed circuit board. In most cases, robot manufacturers, such as Sanyo Seiki, Seiko Electronics, Toyota Machine, Hitachi, and Fanuc, construct their own visual systems for their robots.

But pattern recognition

FRUITFUL IN
TANTALUM CHIP



Which do you pluck?



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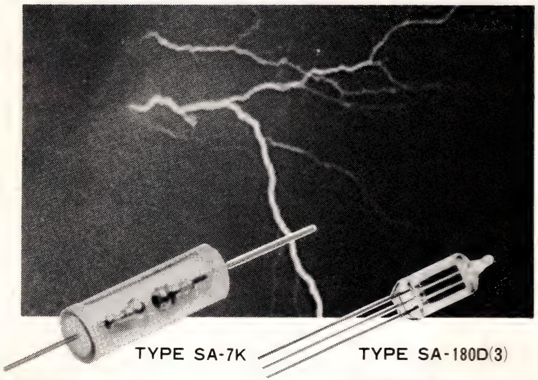

● *TYPE*

Type	Breakdown Voltage (V) DC	Insulation Resistance (Ω)	Maximum Surge Current (8×20us) KA	Life Times at 500A
SA-80SS	80±10%	10^{10} min	1.0	1000
SA-200SS	200±10%	10^{19} min	1.0	1000
SA-80	80±10%	10^{10} min	1.5	1000
SA-140	140±10%	10^{10} min	1.5	1000
SA-200	200±10%	10^{10} min	1.5	1000
SA-250	250±10%	10^{10} min	1.5	1000
SA-300	300±10%	10^{10} min	1.5	1000
SA-7K	7000±1000V	10^{10} min	—	5000
SA-10K	10000±1000V	10^{10} min	—	5000
SA-180D(3)	180±10%	10^{10} min	2.5	1000

SA-180D(3) is a three electrode discharge tube.
All tubes can be made dark effect redused types which are available upon request. D is added to the model number, as in SA-80DSS.

● *POINT*

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(2)Visibility for operation.
(3)Compact and easy assembly.
(4)Stable characteristics.

● *APPLICATION*

Computer circuit.
Communication equipment.
Home Appliance.
Aircraft and Automobiles.

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applications are not limited to factories. Businesses use pattern recognition technology to convert typed manuscripts and lists of numbers into computer data. Also important are image scanning systems that convert mechanical drawings into computer files. Architects, engineers, and even clothing designers use the technology to transfer hand-produced floor plans, blue prints, circuit diagrams, maps, and dress patterns from paper to magnetic disk. NEC, Toshiba, and Mitsubishi Electric all produce such systems, as do Ricoh, Fuji-Xerox, and Nippon Seiki, and Nippon Steel is marketing foreign-made systems to the Japanese market. Still to come are systems accurate enough to read and determine the precise dimensions of machine components and other high-precision parts and applications.

Character recognition systems were probably the first variety of pattern recognition technology to find practical use in Japan when the Ministry of Posts and Telecommunications began using postal code readers in its post offices several years ago. Since then Toshiba Corp. and others have have produced and marketed character recognition systems for use in offices and elsewhere. But these are mostly based on the English alphabet and arabic numerals, and systems capable of recognizing Japanese characters have been slow to materialize.

Larger-scale integration of computer chips has helped to cut the cost of basic character recognition systems so that such systems as the Handy Word Processor, marketed by a small company called Plus, are now available. These systems provide personal computer users with inexpensive character recognition hardware and software.

More ambitious work on the leading edge of character recognition technology is being developed by Tokyo University and the public broadcasting network, NHK. Using neural network models, researchers have found they can produce very high recognition rates, and have attracted the interest of two of Japan's giants: NEC and Mitsubishi Electric.

Japan's Pattern Recognition Markets: Both Steady Growth and Stagnation

Equipment type	1986 (millions)	1987 (millions)	1988 (millions)
Robot systems (that use pattern recognition equipment)	$ 1,840	$ 2,000	$ 2,240
Inspection Systems	360	400	400
Optical Character Readers	136	176	208
Vision Systems	72	80	80
Total	2,408	2,656	2,928

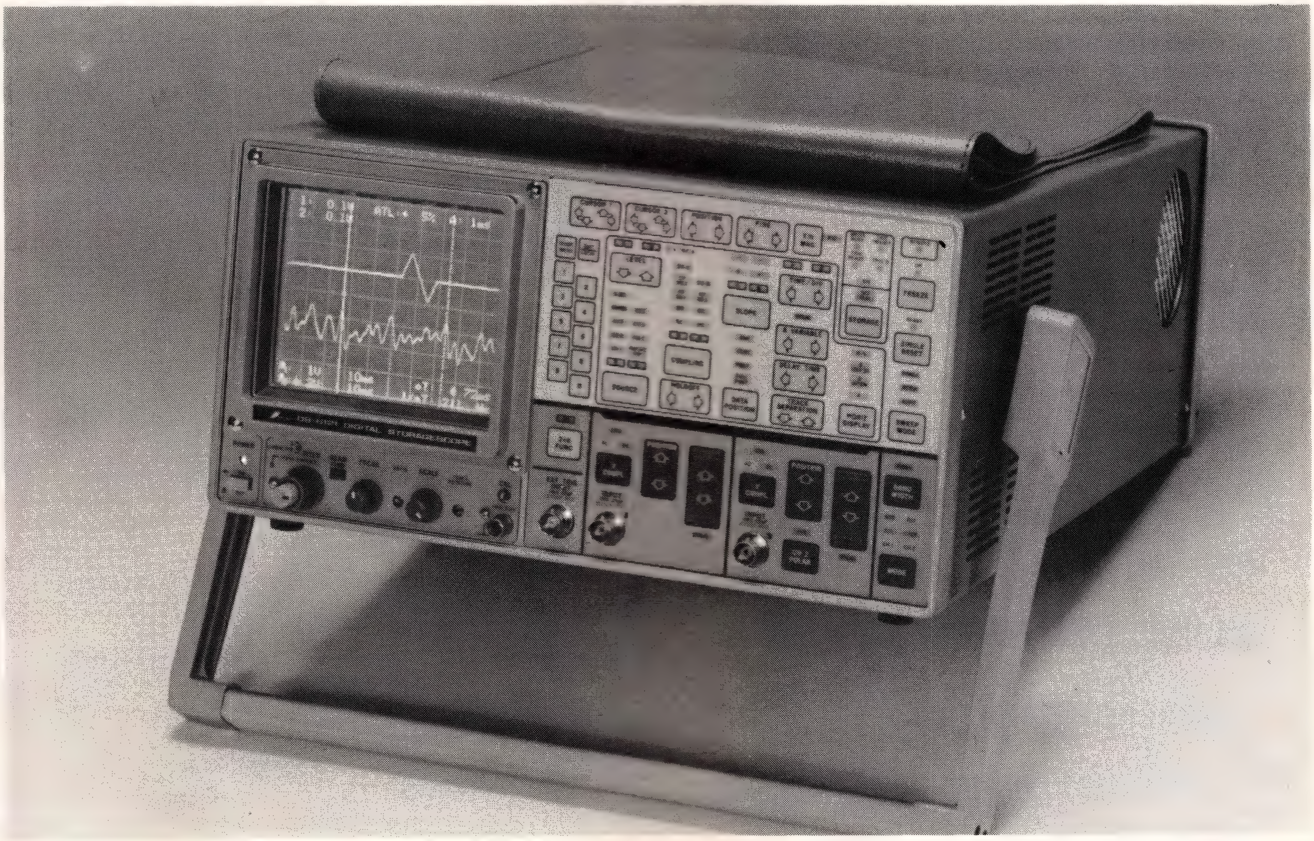
A MARKET COMES BACK TO LIFE

These have been a tough few years for makers of test and measurement equipment in Japan. The shocking downturn in the semiconductor industry in 1985 and '86 wounded the test and measurement industry with aftershock reverberations in '86 and '87, and the rising value of the yen against foreign currencies added to the gloomy picture.

In essence, the industry stood still for two years, according to statistics compiled by Japan's Ministry for International Trade and Industry. Total 1987 production came to $1.87 billion for test and measurement equipment of the electrical variety—roughly the same as 1986—while sales of equipment for laboratory use sunk 2.6% from 1986 to about $800 million.

Now things are looking up. Capital investment for 1988, which plummetted during the semiconductor downturn, is on the rise again, up 40% over 1987. That's good news to test and measurement companies, as the rate of capital investment is a major determining factor in the health of their industry. Buoyed by this and other factors, the market for their equipment is riding a strong upswing and is expected to grow by a healthy 10% this year.

Among the hottest growth areas is optical test and measurement equipment. The increasing use of optical fiber communications in connection with NTT's trunk circuits and local area networks is one reason



New equipment like this 40-million samples/s Iwatsu DS-6121 digital scope is helping to spur Japan's test and measurement market. The unit has a 10-MHz single-shot bandwidth.

for the boom. Other factors at play here are the booming production of compact disks and compact disk players, increasing use of laser disk video technologies, and the rise of optical media as a practical solution for data storage.

The main items in question are optical power meters, optical transmission characteristic measurement devices, obstacle tracing and detection receivers, optical spectrum analyzers, and transmission band characteristic measurement devices. An investigation conducted by the Optical Industry Association found that the market for optical test and measurement equipment, including equipment bound for use in testing optical fiber lines and other buried facilities, amounted to $260 million in 1987, up 22% over 1986.

The new optical spectrum analyzers are capable of simultaneously measuring a wide-ranging photowavelength spectrum intensity. So they can be used to measure not only the line-width of semiconductor wavelengths and the oscillation wavelength of light-emitting diodes, but also the plasma light emission in semiconductor manufacturing processes. As such, they are rapidly making inroads into territory that in the past was exclusively covered by conventional analyzers.

SALES ARE UP ALL ACROSS THE T&M INDUSTRY IN 1988

Transmission band characteristic measurement devices are used to determine the transmission capacity in fiber communications. The operation is highly sophisticated and consists of modulating two or more light sources with different wavelengths; by comparing the sine-wave signals, both the group-delay and the dispersion characteristics for the optical fiber's phase gap can be determined.

Once dominated by Anritsu and Ando Electric, this segment of the test and measurement business is beginning to attract new competitors. Advantest, Shimazu, Sanwa Electric, and others have all joined the fray, itensifying competition.

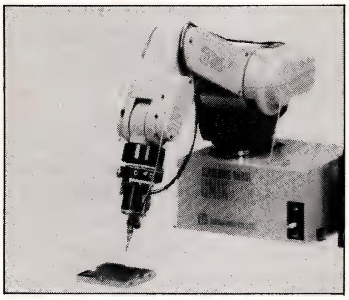
Equipment used to measure electromagnetic noise or interference is also enjoying a sales upswing. This coming December, the Association for Voluntary Control of Computer-related Interference (VCCI), a group consisting of the Electronic Industries Association of Japan and three other industry groups, is scheduled to put in motion a set of measures aimed at voluntarily controlling EMI emissions. The goal is to provide voluntary regulations similar to the mandatory regulations enforced in the U.S. by the Federal

Japanese Test & Measurement Companies: Operations Abroad

Country	Company	Products
USA	Yokagawa Electric	Flow meters, instruments, other meters
	Advantest	LSI testers
	Okazaki	Thermocouples
	Shimazu	Meters and analyzers
	Anritsu*	Optical measurement equipment
S. Korea	Yokagawa Electric	Recorders, controllers, control systems
	Fuji Electric	Coulometers
Taiwan	Kikusui Electronics	Oscilloscopes
Singapore	Yokagawa Electric	Comprehensive instrument control systems
China	Yokagawa Electric	Instrument panels
India	Yokagawa Electric	Comprehensive instrument control systems
Brazil	Yokagawa Electric	Electrical meters
	Fuji Electric	Industrial meters
UK	Anritsu*	Optical measurement equipment
W. Germany	Shimazu	MEasurement and test equipment

* planned

UNIX-521 – The latest in soldering robot development surpasses the skill of experts.



The UNIX-521 is the newest soldering robot developed to reflect the data and know-how accumulated by soldering technicians over many years. It is the result of extensive analysis of the three main elements of soldering: the soldering-gun bit, heater, and soldering material. This robot offers an optimal mix of latest advances in software and hardware with a high degree of perfection.

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Communications Commission. Companies are taking this action to rectify interference problems caused, for example, by automatic transmission systems installed in cars that cause radio reception trouble nearby.

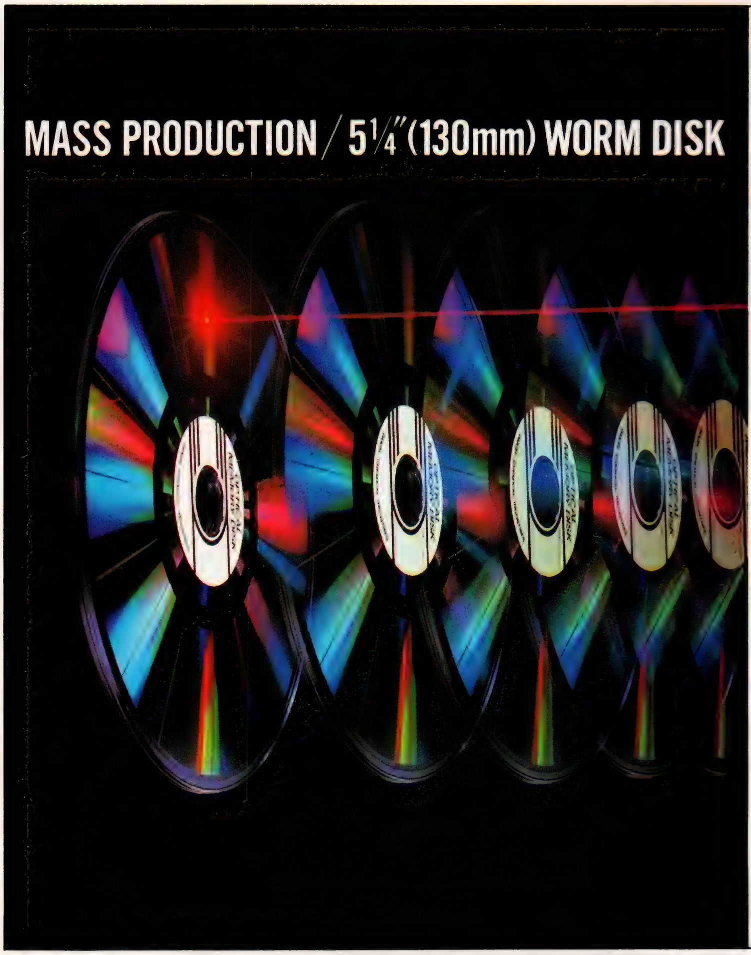
The new rules mean that communications and information euipment manufacturers, as well as radio research organizations and automobile makers, will have to acquire facilities for noise testing in order to live up to the new rules. That translates into a huge expansion opportunity for makers of such equipment, a market that was already worth $77 million in 1987. TDK, Daiwa Rubber, and Grace Japan sell the bulk of equipment for radio dark rooms, a major part of this market segment. Tohoku Metal Industries dominates the market for open-field test sites, another major market sector. These systems consist primarily of spectral analyzers or interference/radio-wave intensity test receivers coupled with noise measurement systems.

NEW RULES FOR EMI SPELL OPPORTUNITY IN T&M

The market for dedicated systems used to measure the performance of specific types of electronic equipment and systems is also growing quickly. These systems, which can be effectively used for a variety of purposes in research and development, manufacturing, and maintenance, include comprehensive measuring systems, for communications and audio visual equipment. The leading manufacturers include Ciebank, Anritsu, Ando Electric, Matsushita Communication Industrial, YHP, and Japan Radio.

Sales of equipment in this market sector reached $88.5 million in 1987, up 13% from 1986. The market is expected to expand further this year, driven by network analyzers, which are essential to the design of high-speed, high-frequency radio communications equipment; protocol analyzers, which are needed to measure transmission signals in communications systems, such as local and wide-area networks; and by equipment for measuring the output characteristics of optical disks.

These hot markets combine with a surging advance in



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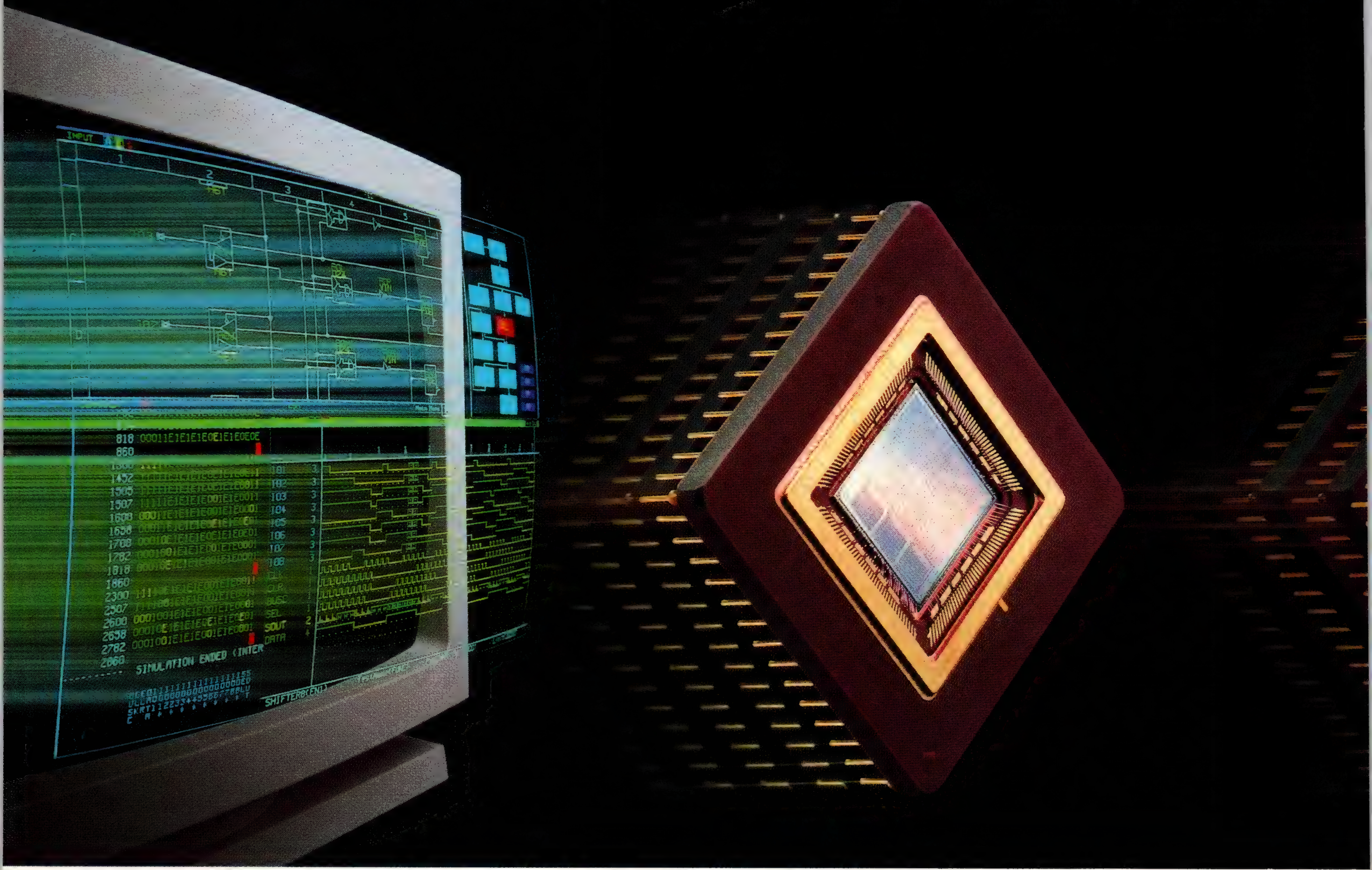
3 reasons Fujitsu ha than anyone else i



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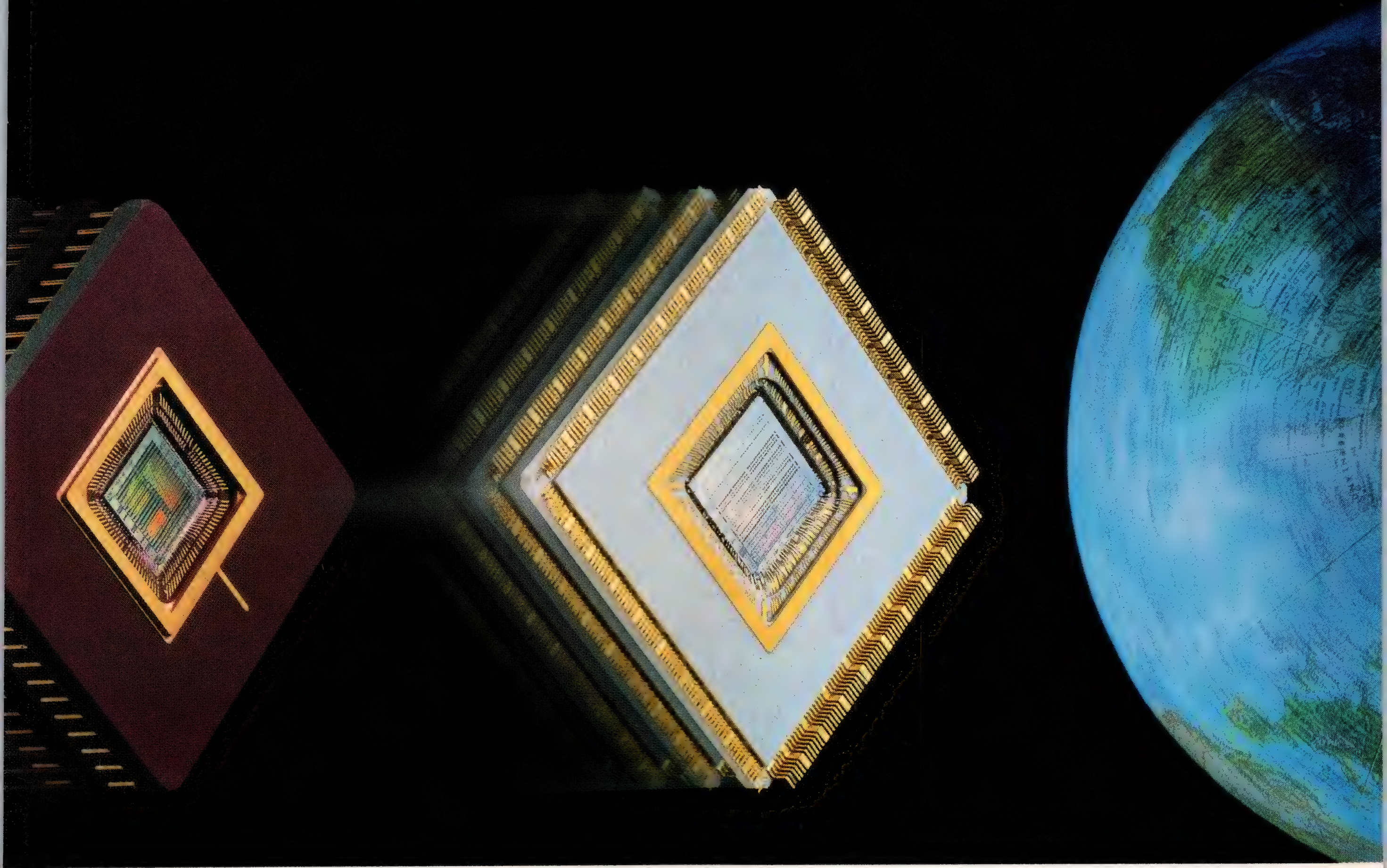

CMOS GATE ARRAY				
Device Name	**Complexity**	**Speed**	**Maximum Signal Pins**	**Typical Power Dissipation**
C-30KAU～C-100KAU	31500～102144	0.6ns/gate	178～332	0.8～1.6 W/chip at 10MHz
C-330UHB～C-12000UHB	336～12734	0.7ns/gate	60～220	50～300mW/chip at 10MHz
C-20000UH	20160	1.0ns/gate	220	500mW/chip at 10MHz
C-15006UM/ **C-10012UM**	15120 w/6K RAM 10080 w/12K RAM	1.0ns/gate TAA: 15ns	219	500mW/chip at 10MHz
ECL GATE ARRAY				
ET-10000H	9856	100ps/gate	200	10～13 W/chip
ET-750～ET-4500	768～4480	220ps/gate	64～128	2～10.2 W/chip
ET-2004M～ET-3004M	1920～2880	220ps/gate TAA: 4～5ns	120	8～10 W/chip
BiCMOS GATE ARRAY				
BC-12000H*	11968	420ps/gate	160	2.5～5.2 W/chip
BC-400～BC-2000	645～3240	550ps/gate	52～112	0.25mW/gate at 10MHz

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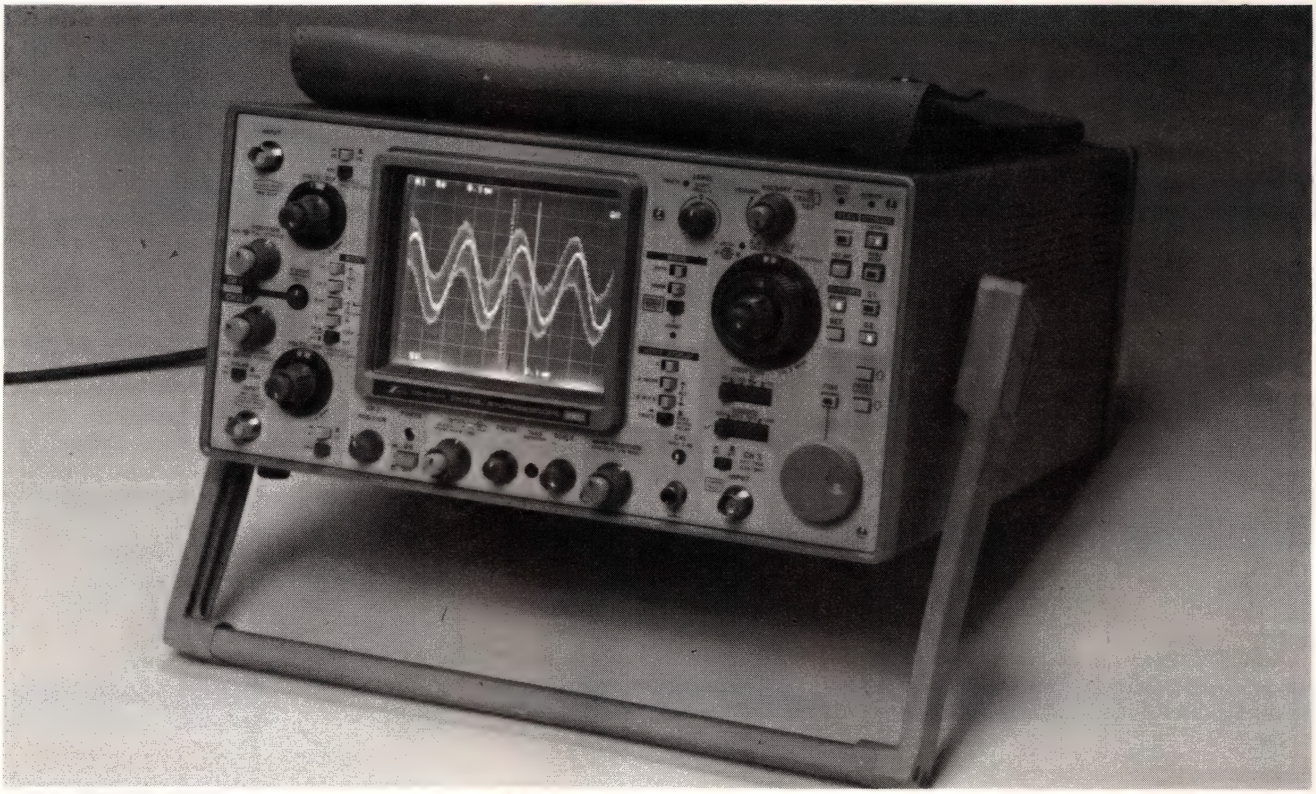
technology to set the stage for an exciting period in the history of Japan's test and measurement industry. Advances in test and measurement technology are generally proceeding on two fronts: functional enhancement and system integration. The rising use of microprocessors is leading the way to more intelligent equipment and software that can draw on artificial intelligence techniques, improving efficiency and functionality.

At the same time, there is an increasing tendency among manufacturers to link various pieces of equipment together into fully integrated systems. This approach provides better efficiency, manufacturers say, since test equipment for communications systems can be combined with audio visual test systems to create a single piece of equipment that can test an entire system on its own. This will be a key strategy for the 1990s.

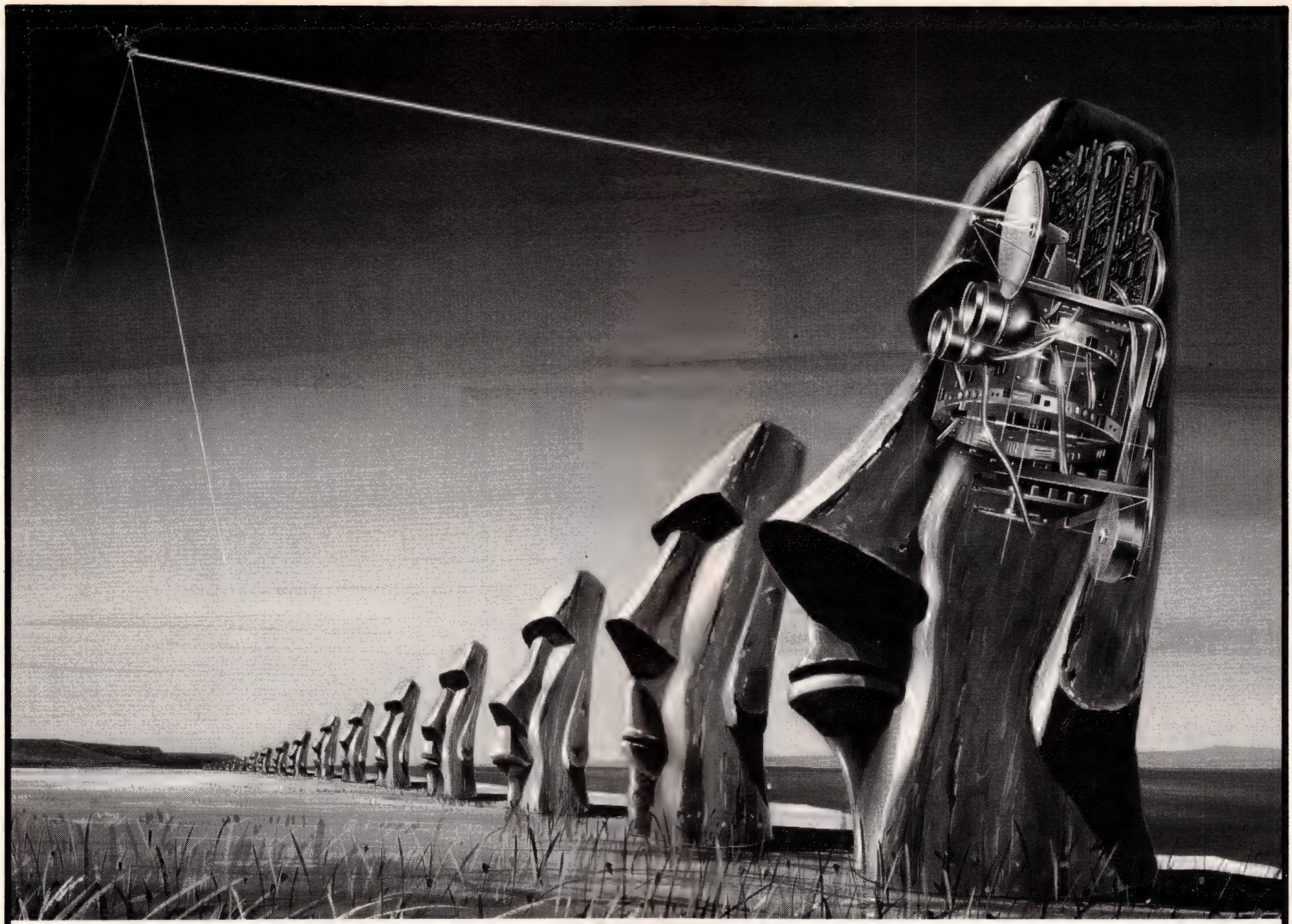
Test & Measurement Equipment in Japan: A Five-Year Study

			($ millions)		
Industry Segment	**1983**	**1984**	**1985**	**1986**	**1987**
Electrical	1,629.7	2,226.5	2,605.3	1,869.6	1,870.6
Digital Multimeters	47.4	66.5	70.2	58.7	62.3
Oscilloscopes	171.2	200.2	213.3	150.2	128.7
FFT analyzers	N/A	N/A	14.3	13.1	12.7
Distortion testers	50.7	70.7	79.7	63.9	63.9
Logic analyzers	N/A	N/A	40.1	32.0	21.4
MPU-related	N/A	N/A	72.7	73.6	49.3
Other	61.5	71.8	86.9	60.9	71.0
Optical					
Transmission-related	169.2	245.1	217.2	396.7	496.8
Test	N/A	128.4	159.4	168.5	206.9
Attached equipment	23.4	35.7	38.6	44.0	53.4
Laboratory Use					
Analyzers	654.3	725.0	856.9	822.3	800.5
Photoanalysis	181.9	209.5	236.2	216.0	203.5
Electromagnetic analyzers	128.9	138.3	159.1	152.3	144.4
Chromatic/separation/ distillation	123.6	138.8	174.3	221.3	159.3

Source: Ministry of International Trade and Industry, Optelectronic Industry and Technology Development Association.



Iwatsu's DS-6411 digital storage oscilloscope, which samples waveforms at a 10-million samples/s rate, is another example of new test and measurement equipment coming to market from Japanese suppliers.



Technology for the Future.

One of the world's great mysteries···the monoliths of Easter Island. Who built them ? For what purpose ? And how were these 90 ton giants constructed ?

Some say these unique, stone structures were used for esoteric religious rites. Some even say they were built by beings from another planet. Perhaps we will never know for sure. One thing we do know, however, is that the constructors had advanced technology for their time.

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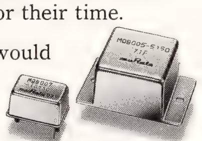

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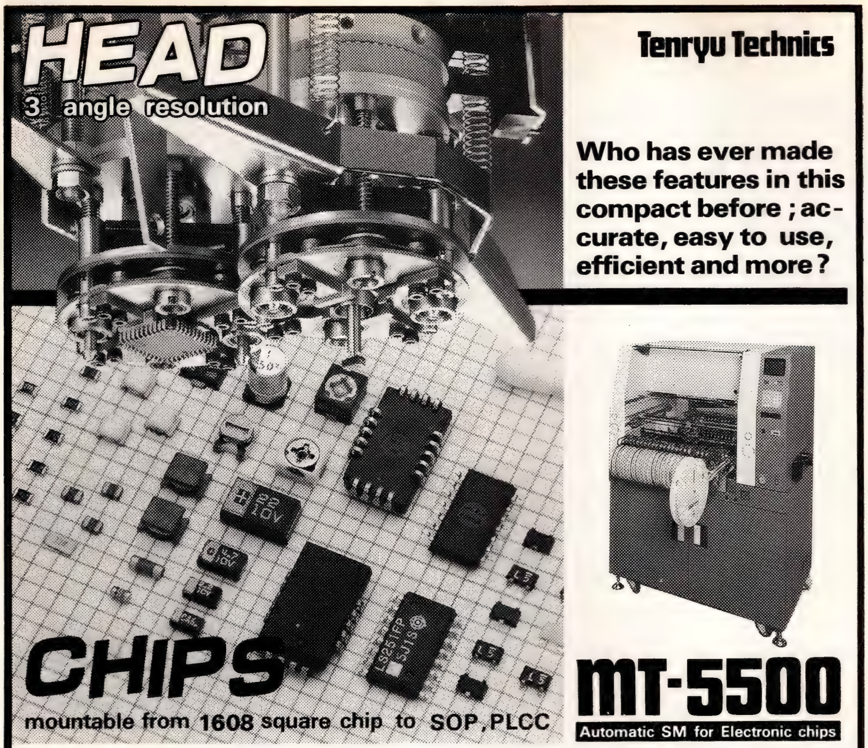
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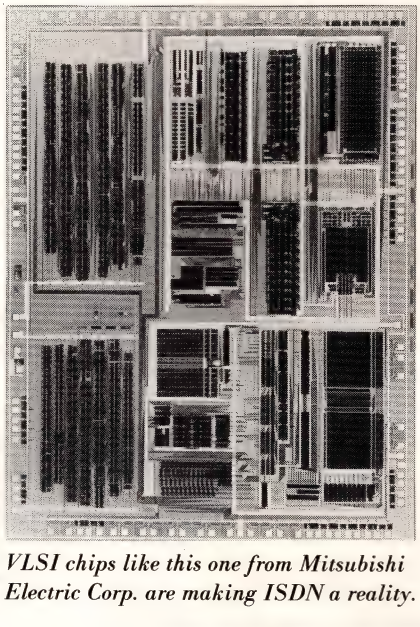
TELECOMMUNICATIONS

JAPAN GETS READY TO IMPLEMENT ISDN

The Integrated Services Digital Network is alive and kicking in Japan.

NTT started its ISDN service—INS NET 64—in April, and Japan's telecommunications industry is fully geared to the ISDN environment. For now, the service is only available in Tokyo, Nagoyo, and Osaka, but the service area will be expanded to cover all the major cities by the end of next year. And INS NET 1500, a high-speed 1,500-Kbits/s network, will start operation next year, NTT officials say.

In addition to the standard features of ISDN, such as multimedia and multi-channel communications, and high-speed and quality, the INS Nets will provide customers with a variety



VLSI chips like this one from Mitsubishi Electric Corp. are making ISDN a reality.

When ISDN Services Go On-Line in Japan

Year	Service
1988	* 64-Kbit/s ISDN circuit switching * Satellite communications * Multiplexed FM radio broadcast <M-> tests service begins in Tokyo.
1989	* 64-kbit/s ISDN packet switching * 1.5-Mbit/s ISDN circuit and packet switching * Teleterminal systems become available
1990	* Broadcast satellite * High-definition TV
1992	* ETS-VI: multibeam staellite begins technical tests
1993	* Digital cellular redio communications begin
1995	* Broadband ISDN begins

of special features. These include:

- Identification of the calling party by providing the receiving party with the caller's telephone number, which would be displayed on a phone-mounted monitor;
- Notification of the cost of service immediately following communication, by displaying the price on the caller's monitor;
- Notification of incoming calls call during communication, a service not unlike today's call-waiting services;
- and the ability to leave a message or to use a password of up to 128 characters in length when the party being called is busy or otherwise unavailable.

NTT expects to have 100 service areas in operation by 1990, with 100,000 lines connected. Then, beginning in the early 1990s, NTT will begin to test broad band ISDN. NTT is developing CTRON, an operating system for communication control, that it plans to use in future INS Net offerings.

NTT, in conjunction with Japan's Ministry of Post and Telecommunications, hardware manufacturers, and information and communication service companies, is studying a variety of services that could be delivered through an ISDN. These include the video telephone, message handling services, telex and facsimile transmissions, video teleconferencing, still-video teleconferencing, multi-media packet switching that could permit higher priority for voice transmission, electronic voice mail, stereo digital audio transmission, digital videotext, full color facsimile, and high-definition television.

All of this has attracted NEC, Fujitsu, Hitachi, Toshiba, and Oki Electric to betgin developing products for the coming ISDN market. These products include digital multi-function telephones, video phones, multi-media multiplexers and other products.

The Ministry of Post and Telecommunication has established a Terminal Equipment Development Committee to develop ISDN terminals, and that committee has already turned in a report on how best to handle the problem. The committee seeks three categories of terminals, and would set up separate specifications for home, office, and public use (see chart).

Home terminals would include basic models for home security and voice and data communications; a video telephone; and more advanced, multifunction terminals that might combine personal computer features with those of an ordinary phone to allow users to access video text services, for example. Eventually, a still more advanced home phone system would enable users to enjoy broadband image communications.

Business terminals would not be much different. Video phones,

What Kind of Terminals Will ISDN Support?

Location	Type of Terminals
Home	* Basic telephone terminal for home security and communication. * Video telephone. * Multi-function terminal integrating personal computer and video text functions with the basic terminal. * Advanced function terminal providing boradband image communication.
Business	* Voice terminal. * Facsimile terminal. * Video terminal with integrated voice communications. * Document production terminal. * Document retrieval terminal.
Public	* Digital public telephone. * Data retrieval terminal. * Facsimile terminal. * Public video telephone terminal.

facsimile machines, and terminals for document production and retrieval could all be supported with ISDN capabilities. ISDN isn't the only communication field heating up. Mobile communication is also picking up steam, and is getting a big push from the introduction of satellite communication carriers that will support both voice and data communication. Eventually, NTT hopes to tie these services in with its ISDN implementation.

Japan's Telecommunications Market Keeps Growing at Its Own Easy Pace

Type of System	(millions) 1986	1987	1988
Customer premise equipment	$ 1,623	$ 1,736	$ 1,846
Private voice and data switches (private branch exchanges)	501	552	625
Public voice and data switches	1,152	1,354	1,433
Transmission and carrier equipment	2,262	2,374	2,502
Total	5,538	6,016	6,406

KODENSHI: JAPAN'S OPTICAL CHIP LEADER

Hirokazu Nakajima, President

KODENSHI Corp. is the largest photoelectronic semiconductor specialist in Japan. With over $7 million invested in capital equipment and space, the 16-year-old company has a stable track record and recorded sales in excess of $48 million for the fiscal year ended March 30, 1988.

KODENSHI's presence is still largely based in Asia and the Pacific Rim, but now the company is looking to North America for expansion and future growth. The aim is to find markets for its optical sensors and unique manufacturing capabilities—KODENSHI brags that its production facilities in Kyoto, Japan, are so versatile it can respond to orders as small as a single custom-unit and as large as a full-scale production run.

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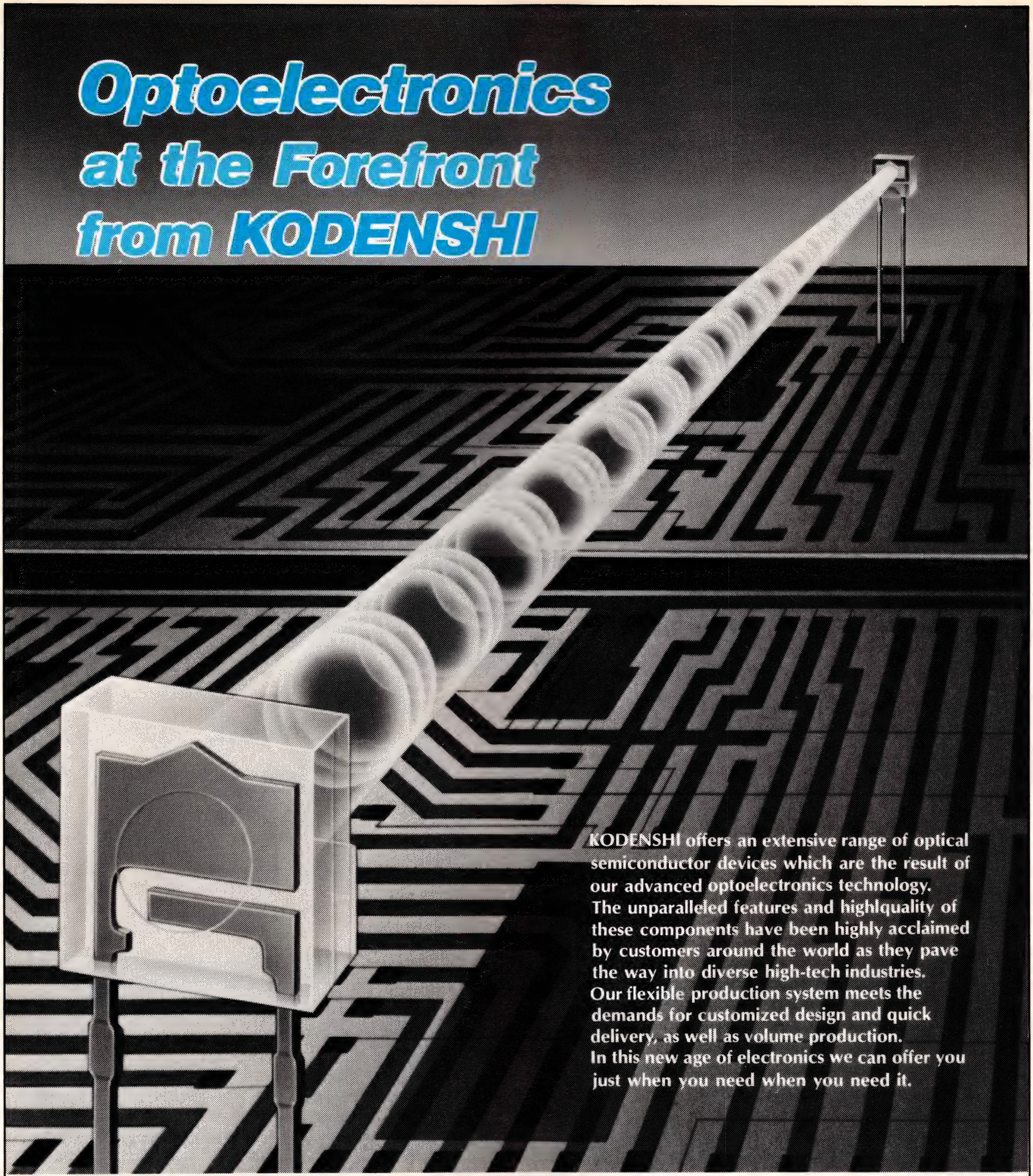

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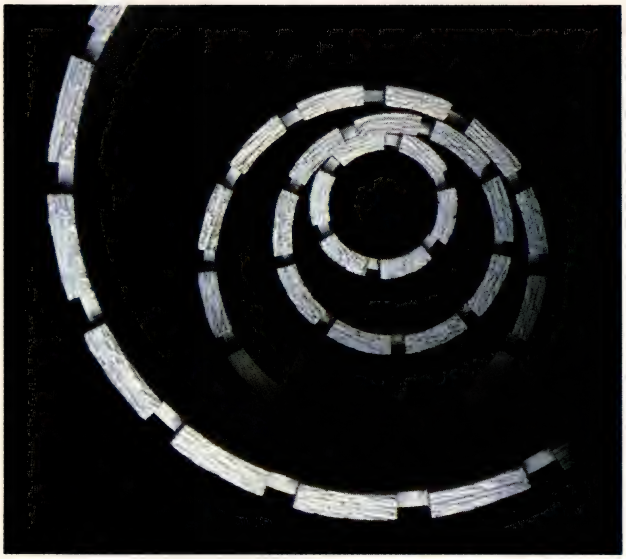

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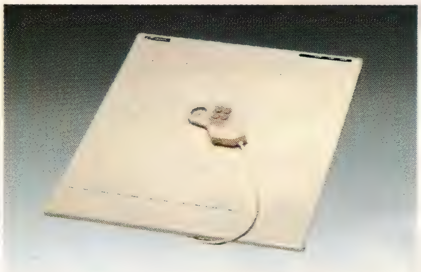

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'DID I SAY QUOTA? I'M AFRAID I DID'

For semiconductors, or any products or services, protectionism doesn't work if it's applied as a rule directing world trade. It ultimately stifles growth and trade volume and brings depression. But it certainly works for a single country that uses it in a concert of nations that don't.

Protecting a market or a nation is certainly proper under specific circumstances—one is when the nation is under development and doesn't have the strength to play in the major leagues; another one is to protect the system when a country is not playing by the rules that govern free trade. Now lets look at the U.S.

Lee Iaccoca pointed it out first; in certain respects we are reverting to a colonial status. Let's take a look at some of those respects: We export raw material and commodities (minerals and agriculture) and import finished products. Not only are we importing the products with the most value-added but in the process we have managed to incur a trade deficit year after year for more than a decade. This deficit is concentrated in one country—Japan.

The dollars from Japan's export surplus are being invested in the U. S. through government securities, factory building, and real estate purchases. These investments are starting to put pressure on our economic freedom. For example, interest rates have to be kept artificially high to keep the flow of money coming in and the value of the dollar stable.

With Japan owning more and more of this country, we are used as mercenaries to defend the empire without controlling it, and in the process spending in excess of $200 billion. This forces us to run a budget deficit. As a result of the trade and budget deficits, our currency is no longer under our control, and the Federal Reserve System leverage against the amount of dollars controlled overseas is lopsided.

The U. S. is now a net debtor nation like Argentina or Mexico; we owe billions of dollars to foreign nations. Capital formulation, or the saving rate, is very low by comparison to the country that is in control, allowing a gradual takeover of the productive assets in this country.

Our economic strength is eroding like a beach, grain by grain. Clyde Prestowitz notes in his book *Trading Places* that when the Japanese invest in the U. S. they use Japanese construction and engineering firms, money from Japanese banks, and Japanese contractors. This creates a completely segregated world where management is not integrating the indigenous population. When the company goes into production, it does so only with Japanese management directing the assembly of modular parts coming from Japan.

DANIEL QUEYSSAC

Age: 48
President, CEO of SGS-Thompson Microelectronics Inc., Phoenix
Career path: President of SGS Semiconductor Corp. before 1987 merger with Thompson Components-Mostek Corp. Former manager with Motorola Inc. during the 1970s.

QUEYSSAC'S STANCE:
"The U. S. government should step in to protect our markets."

This trend typifies a colonial environment where the colony is used only for labor, not for design. This practice creates more markets for Japanese products, cutting down the U. S. manufacturer's share of the home market.

The examples of televisions or automobiles are cases in point. When a Japanese company operates in the U. S. it uses Japanese components, as in the case of automobiles in this country. In fact, if Japanese companies buy anything locally they try to buy it through Japanese-owned firms, or they encourage Japanese subcontractors to set up shop in the U. S.

In order to accomplish all this the Japanese have allocated a lot of resources to develop a massive lobbying power that has already had major impact on many political decisions made in this country.

Finally, one of the last aspects of the colony-master relationship is the disparity of cost of living, where everything is cheap in the colony. This certainly applies to the U. S.-Japan relationship. At this stage the solution is political; it is no longer industrial.

The industries of this country cannot change the situation if the overall economic environment doesn't change. In order to correct the capital formulation problem and dampen the consumption encouraging the trade deficit, we should move from an economy of consumption focused on today to an economy of savings looking toward tomorrow. This can be achieved very simply by a shift in the philosophy of taxation. Savings should not be taxed and consumption should be. Use a global excise tax.

This will certainly take a long time to decide and to produce an impact. In the meantime, we need government intervention as far as our industry is concerned. When, in a game, a player or a team doesn't follow the rules, the referee intervenes to penalize the culprit and reestablish fair play. And already in the U.S., we are seeing our ranks being diminished. If you look at the consumer business in this country, it has basically disappeared. I think the next to go will be computers and telecommunications, although they might take a little longer. Something has to be done beyond the fair market-value agreement covering a few products and the Sematech effort—and it has to be done by the government.

After countless unsuccessful tries to pry open the Japanese semiconductor market, it is clear that the solution will not be brought about by any more negotiation. We need to establish a quota for Japanese semiconductors coming into this country. Our quota should be established to give the Japanese the same percentage of our market that

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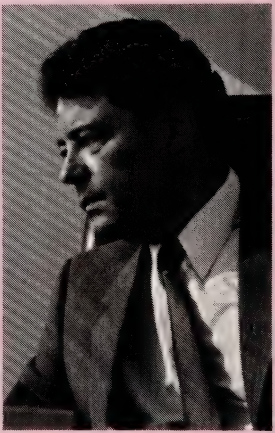
they give to us of their market.

This quota should also include Japanese semiconductor products imported inside of finished products. Although there may be a short-term problem created for end users, it will be more than offset by the long-term advantage they will derive from a very strong national industry.

It is time to take action to protect our technology while it still exists and has the potential to grow again. If we make the mistake of letting it perish, it will be lost forever. "Semiconductors" will become the latest entry on the long list of industrial capabilities that have disappeared from the North American continent.

Q *ELECTRONICS:* You believe protectionism is dangerous if used worldwide as the "rule directing world trade," but that it can be constructive when used by one country to offset imbalances with a specific trading nation. Doesn't that position risk perpetual protectionism?

A QUEYSSAC: Yes. So what needs to be done is to make sure that the rule of the game is free trade. I think the only way to give an incentive to people to play by the rules is to say that as long as you exercise free trade we will do the same and to make sure that for a comparable-size economy—which happens to be the case between the U. S. and Japan, in terms of GNP revenue per head—that there is the same percentage of trade going both ways. If there is a disparity, it should be corrected by preventing the other one from taking advantage of it.



There may be some small difference in the electronics trade balance because of specialization of one country vs. another, but certainly in overall value we need to make sure that there is not a systematic and huge trade deficit developing year after year.

Q *ELECTRONICS:* You are advocating taxes to shift the U. S. economy from one that is consumption-driven to one with more emphasis on savings. How?

A QUEYSSAC: What we are talking about is basically a value-added tax, but one that is taxing consumption, not encouraging consumption.

Q *ELECTRONICS:* But isn't there a danger of choking off electronics markets?

A QUEYSSAC: I don't believe so. We are not talking about creating new taxes, just shifting tax from savings to consumption. This would reinforce the move to phase out write-offs of interest paid on loans and credit cards. You would have a value-added tax which would allow you to capture a lot of transactions in the economy that are not now directly taxed.

Q *ELECTRONICS:* So, you believe the shift to a savings-minded country will help the U. S. in trade by lowering the interest rates with available capital. In the meantime, you believe trade quotas on the Japanese semiconductor houses are needed to create a level playing field for U. S.-based semiconductor companies. How would you administer those quotas?

A QUEYSSAC: It has to be a percentage. We need to have the freedom to import what is needed. But in terms of value, we should set a limit. We should say: "Here's what [dollar amount] the Japanese are buying [from the U. S. suppliers] and it is what we will buy from them." We need to try to establish an equilbrium.

There is always a good excuse for them not to buy the product—it is not ready, not the right quality, not the right service, or we are not talking Japanese. There is always some good reason, so you have to give them a very positive incentive.

Q *ELECTRONICS:* Many of the Japanese firms have created U. S. operations. Would you encourage those moves?

A QUEYSSAC: There is no problem if companies want to come here. But we must discourage them from coming here, manufacturing here, and still importing all of their products [components]. All they are using from here is the local labor.

Q *ELECTRONICS:* So this gets back to the point about the U. S. becoming more like a colony.

A QUEYSSAC: Yes.

Q *ELECTRONICS:* SGS-Thomson Microelectronics Inc. is a U. S. subsidiary of a European-based firm. Would you want to have a distinction between European- and Japanese-based firms?

A QUEYSSAC: There should not be a distinction. It just happens that in Europe there is a reasonable balance of trade. In fact, the trade is in favor of the U. S. As long as there is an exchange, I think it should be encouraged. It is good to try to encourage international trade. It looks like Europe is buying and selling, and there is a good flow in both directions. I don't see any problem there.

Q *ELECTRONICS:* Does Europe need to take these same protection steps?

A QUEYSSAC: Yes. In fact there is a lot of talk in Europe for something similar. ☐

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COMPANIES TO WATCH

CAN APOLLO CLIMB BACK FROM ITS $7.9 MILLION FALL?

Vanderslice hews to plan as analysts fear company will be an also-ran

CHELMSFORD, MASS.

Apollo Computer Inc. is doing just what any company stung by an unexpected $7.9 million second-quarter loss would do—it's groping for answers. And industry analysts say that Apollo may be right in pinning much blame on its West German subsidiary—but they still wonder if it is doomed to take a permanent back seat in the work-station market.

Just the same, don't look for big changes at the Chelmsford, Mass., company. Apollo chairman Thomas A. Vanderslice says it is going to stick with the course he charted a couple of years ago. Vanderslice is beefing up the company's marketing, research and development, and sales departments, adding 50 people in marketing alone. But those are tactical moves, designed to boost sales in the short term, as well as to respond to intense market pressure from Sun Microsystems Inc.

The strategic game plan is to press innovative product development. Apollo's new work stations introduced in July have drawn favorable reaction, although that fact was almost buried by the bad news. Apollo will also continue to aggressively support standards such as Unix, and pursue strategic alliances with customers and third-party software developers [*Electronics,* May 28, 1987, p. 45].

Even as a rebound is planned by Vanderslice, who is also chief executive officer, there are muted rumblings that the work-station pioneer could be a takeover candidate. While a mere year ago he pointedly listed obstacles to an acquisition, now Vanderslice tersely says, "We would do whatever is right for the shareowners and employees."

LONG RECOVERY. Takeover or no, industry analysts say Apollo will need at least two quarters to get back on track following the $7.9 million loss on revenues of $143.5 million in the quarter ending July 2. And the departure of its president and chief operating officer, Roland Pampel, will need fast mending too. Pampel's resignation apparently wasn't directly related to the company's performance. He quickly resurfaced as president and CEO at Honeywell Bull Inc. just days after departing from Apollo.

Vanderslice isn't immediately looking for a successor to Pampel. "I'm back running operations; I'm more closely involved and spending more time on engineering and marketing issues," he says.

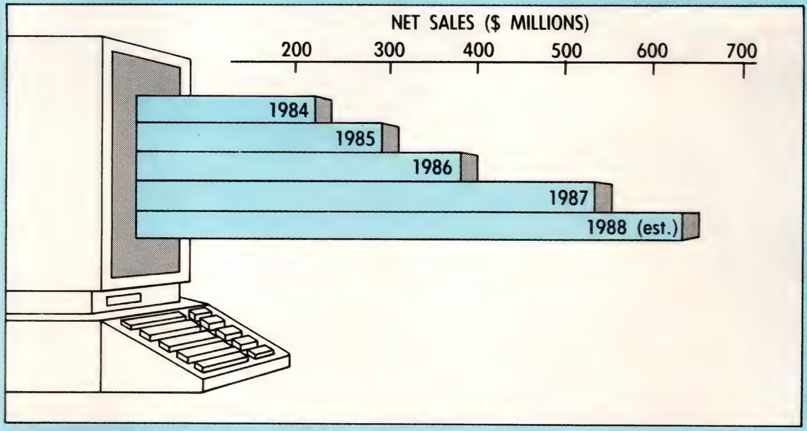
But where were Vanderslice and Pampel when the disastrous shortfall was building in Apollo's West German subsidiary? analysts ask. Much of the second quarter results—which were about $30 million less in revenues than expected—reportedly came as a surprise. The subsidiary's problems are widely believed to stem from Siemens AG's postponing delivery of a $20 million order. Now Apollo has fired its manager in West Germany.

"There's no excuse for [Apollo] not to know" that the systems intended for Siemens were accumulating in inventory, says Vicki Brown, senior analyst for work stations at International Data Corp., Framingham, Mass. And she points out that the work-station market is growing at least five times the 9% rate that Apollo grew in its second quarter. "That's a sad situation for the company that started the work-station business," she observes.

Mark Stahlman, research analyst who tracks work stations closely for Sanford C. Bernstein & Co., New York, says he's convinced that Apollo was truly surprised by the misstep in Germany. "It's difficult not to view this as a major management failure on the part of the German subsidiary," he says. Vanderslice doesn't contest that assertion.

But Vanderslice is steadfast against a drastic cutback now. He points out that Apollo has just completed a three-year switch from proprietary to open-system Unix-based networked computing strategy. "Here we are with a first-class system and an open architecture, but what do I do right now after the second-quarter results? Cut back on people and ex-

APOLLO'S SALES WALTZ ALONG ...



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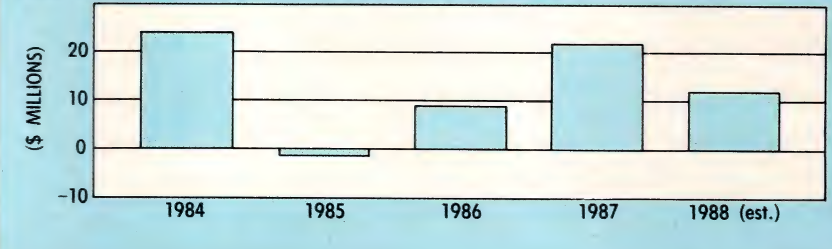


SOURCE: APOLLO COMPUTER

penses? We're not going to do that because when you have the right products and a worldwide infrastructure, you should be more aggressive. We're hiring in critical areas, including marketing, research and development and sales. Will it work? You'll know in six to nine months."

Stahlman thinks the buildup is a good idea, but he says Apollo's problems are deeper than the second-quarter results indicate, stemming from a strategy that will "limit the scope of its business and trigger continued market share loss."

Apollo seems to be content with providing the interconnection between dissimilar hardware nodes on a network, he says, rather than competing to displace those nodes, such as the Digital Equipment Corp. VAX servers in networks. In contrast, Stahlman sees Sun aggressively going after "everything from the $3,000 desktop work station to the $300,000 server. Sun wants to displace the VAXes and sell that whole range," he says.

Vanderslice doesn't deny having a more limited networking strategy. "We see our plate as being very full in work stations," he says, concurring that Apollo is after the interconnection role in networks. And Vanderslice doesn't want to compete head-on with DEC in the minicomputer-class server slot. "This could be a fault, but I don't see us knocking off DEC. We see ourselves penetrating DEC the same way DEC has penetrated IBM."

SUN'S MOVE. At Sun, Edward J. Zander, vice president of marketing and a former Apollo executive, confirms the Mountain View, Calif., firm's shift in markets. "We've taken great pains in the last year to get away from the engineering work station identity in favor of being a general-purpose distributed computing company," Zander says. "We stress the integration of the desktop, server, and network as much as possible."

But Zander doesn't perceive substantial differences in the two companies' strategies. "Apollo's pitch seems to be similar to ours, but we're executing a little better just now. Nobody at Sun is dancing on Apollo's grave."

Meanwhile, almost lost in the noise about the second-quarter Apollo setback is the significance of the desktop Apollo series 4500 and 3500. The 4500 is the first work station to use the 33-MHz versions of the Motorola MC68030 microprocessor At 7 mips, the 4500 almost doubles the performance of the year-old series 4000, says Cheryl Vedoe, director of work station and graphics marketing at Apollo. The lowest-priced monochrome version of the 4500 sells for $19,990. The 3500 uses the 25-MHz 68030 and 68882. A version with a monochrome screen is priced at $7,990, making it the lowest-priced 4-mips work station available, she says.

Stahlman concedes that the 3500 and 4500 "are excellent products and logical extensions of their current product lines." But, he adds that because neither the 4500 nor the series 10000 personal supercomputer [*Electronics*, March 3, 1988, p. 69] is due until later this year—and because the 3500 competes against the series 4000—Apollo is in for a long product transition. *–Lawrence Curran*

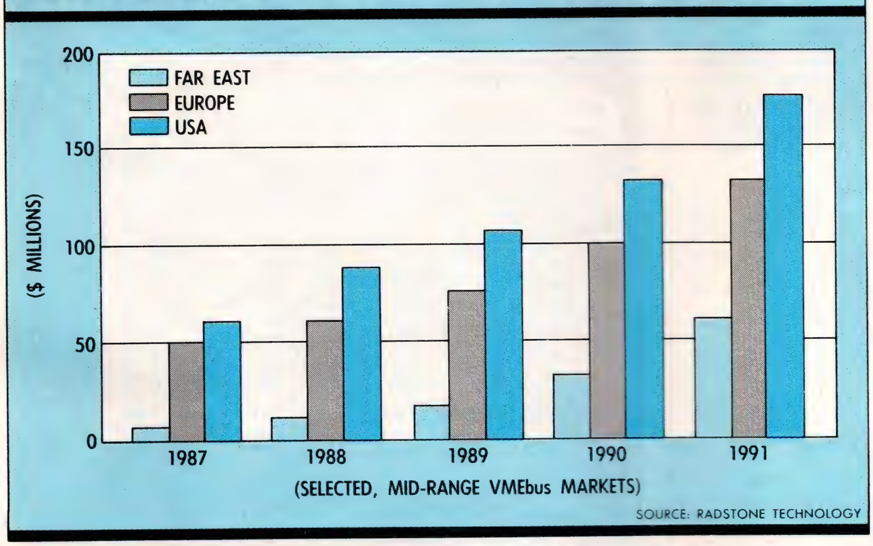
THE POST-PLESSEY GAME PLAN AT RADSTONE

PEARL RIVER, N. Y.

By early last year, the stepchild syndrome was in full bloom at Plessey Microsystems. Six managers were asking themselves whether a thriving, $50 million business in memories, VMEbus boards, and defense subsystems would ever find happiness as an appendage of Britain's Plessey Co. plc, a $2 billion electronics conglomerate.

The answer was no; the solution was a management buyout; the result is Radstone Technology Ltd. Having sprung already mature from its parent, the upstart has targeted an ambitious growth path. Of keen interest to Radstone is the VMEbus board market, which is expected to grow at a rate of at least 30% annually both in the U. S. and Europe. Radstone still has its international headquarters in Towcester, UK, near the town of Radstone, and has its North American headquarters in Pearl River, N. Y.

Once the six mangers decided they wanted to be entrepreneurs, they sent out feelers to Plessey—with considerable trepidation. "One always wonders if they will say 'no' and then fire you," says Chris Doggett, president of the company's U. S. marketing and technical support operation. But Plessey proved receptive and, with the help of UK venture capitalists Investors in Industry Ltd., the deal crystallized in May. Details, including price, have not been disclosed. In addition to Doggett, the buyout partners were Charles Paterson, managing director; Ian Chapple, director of commercial products; Tom Hall, director of military products; Rod Tustain, controller; and Roy Richardson, managing director.


HOW RADSTONE SEES ITS VME NICHE GROWING

SOURCE: RADSTONE TECHNOLOGY

ON THE MOVE. The company had already been on a growth path, particularly in VMEbus boards, after emerging from the pack in 1984 to rack up $10 million in U. S. sales last year. That's enough to put it in third place, nipping at the heels of second-place Force Computers Inc. of Camarillo, Calif. Motorola Inc., Phoenix, Ariz., is the sales leader.

Out of a worldwide VMEbus market, including captive production, of about $340 million in 1988, Radstone is targeting a $155 million market for its commercial systems. This target market can be generally characterized as addressing midrange performance in the 6U form factor, and excluding ruggedized boards and boards fully qualified for military use. It is expected to grow at about 34% per year and reach $365 million in 1991 (see graph).

To get there, Radstone has ambitious product plans. It will introduce products at the Buscon show in October, including and full mil-spec Small Computer System Interface, and memory and central processing unit boards. But a slew of new products is not the limit of Radstone's interests. Acquisitions, licensing agreements, and strategic alliances are all on the menu now. Its new-found indepen-

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dence means "we don't have to depend on organic growth any longer. We can go out and raise money, acquire other companies, and get involved in other businesses,"says Doggett.

Although he won't say what acquisitions may be planned, Doggett says that optical disk technology was an opportunity Radstone might have taken—had it been captain of its own ship back in its Plessey days. The company now supplies original-equipment makers with military and commercial versions of Multibus and bubble memory subsystems, in addition to its VMEbus products.

Doggett is interested in moving more aggressively into the U. S. military markets, an area where Radstone was forced to step gingerly because Plessey plc's presence there required adherence to the corporate line. "It's a vast market, especially for VME," he says, adding that Radstone will now combine its military and commercial product lines under a single marketing plan. Giving customers a full range of commercial and military boards lets them make design prototypes with the less expensive commercial board before qualifying the military version, he says. *–Jack Shandle*

HOW SCHLUMBERGER/ATE HOPES TO BOUNCE BACK

SAN JOSE, CALIF.

Some rival automatic-test-equipment manufacturers like to compare Schlumberger/ATE to an aging rock star who lost his creative edge after turning a deaf ear to his fans. But they might be in for a surprise. The one-time ATE leader is pounding out a new beat in San Jose, Calif., that it hopes will be music to the ears of customers. And it's doing it with a new approach to manufacturing and quality control.

Over the next five years, Schlumberger plans to double the $243 million business it did in 1987, says Irwin Pfister, vice president and general manager. To reach that goal it will have to recoup its shrinking market share, and some help will come from the advanced manufacturing center it opened in Simi Valley, Calif., last month. From that facility, rivals and customers alike will see major annoucements across Schlumberger's product lines beginning in 1989, the company promises.

But the firm, a subsidiary of the multinational oil-field-services conglomerate of the same name, has a long road back. "If you go back to the 1978-79 time frame, the company had 60% share of the entire ATE market," says Dan Hutcheson, president of VLSI Research Inc. of San Jose, Calif. "It was the largest semiconductor test-equipment manufacturer in the world. [At that point the unit was part of the Fairchild Camera & Instrument Corp.] Since then it has continually lost market share (see figure). Between 1979 and 1986, the company has remained the same size while other companies have grown."

Pfister, who joined the company in May 1986, concedes that a big job lies ahead. "We have not made the most effective use of our installed base of customers. We abandoned them on some product lines, but we will be going back and bringing them products that will protect the investment they have made," he says.

By establishing much tighter control of manufacturing, the company plans to reduce costs as it improves quality significantly. "We need to build ATE systems at 30% the cost of systems now being offered," Pfister says. "Customers cannot afford $5 million for a test system. In addition, the system must be very reliable to minimize down time. You can achieve this combination through advanced manufacturing techniques."

The vision of a fully automatic factory is far from the reality embodied in the Simi Valley facility. Automation and capital equipment are being used to improve quality—not to increase productivity per se. "We use the term 'advanced manufacturing center' to imply advanced concepts and techniques rather than robotics and automated guided-vehicle systems," says Tom Weiter, vice president of operations.

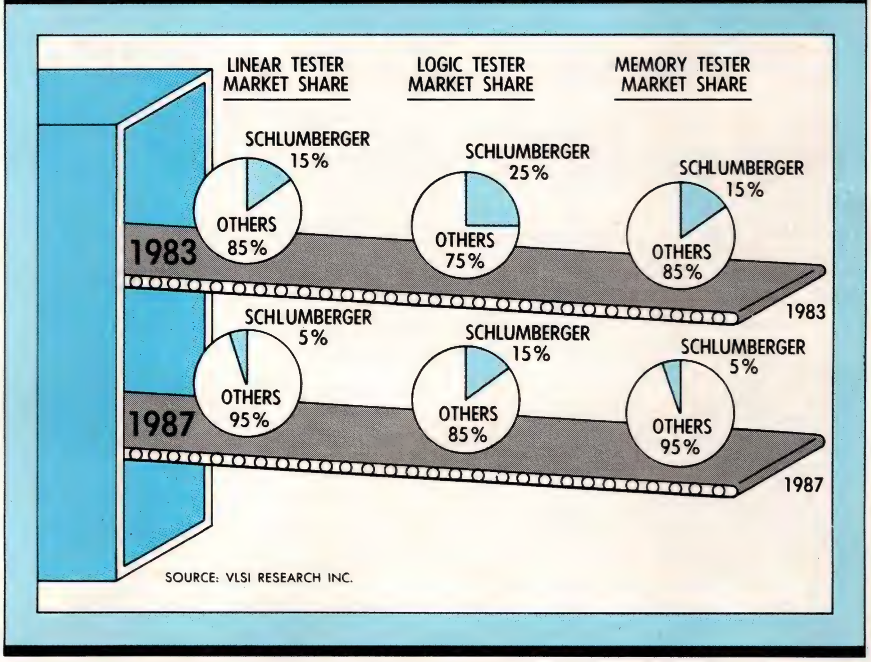
To find the optimum combination of productivity and quality, Schlumberger is analyzing its manufacturing process at a much more detailed level than in the past. The firm has devised what it calls a "focused-factory approach," whereby overall objectives will be drawn from specific goals for individual work cells each month. These aims will be based on meeting cycle times and customer commitments in a timely manner, monitoring scrap and rework costs, watching how quickly inventory is turned over through a cell, and other factory variables.

And the target isn't just costs: quality control also has a high priority. A shop-floor data-collection system collects failure-rate information at key points in the manufacturing flow and performs statistical analysis to find out what components are failing and what workmanship problems are causing the failures.

"Two years ago it was possible that several boards could have been produced incorrectly before the fault was caught," says Pfister. "Today if one board has a problem, the line stops until the problem is identified. By shutting down the production line, the problem gets immediate attention." The system has many elements of Japanese "just-in-time" practices.

But a state-of-the-art manufacturing center is useless if there are no new products to produce. To address this problem, Schlumberger will announce some new products before the end of the year, fruits of its long-term research and development program. What to expect? Here's one hint: "The IDS 5000 [a tool to debug prototypes] is a good example of new technology that will be coming out," Pfister says. *–Jonah McLeod*

ATE FRONTRUNNER'S MARKET SHARE DWINDLES



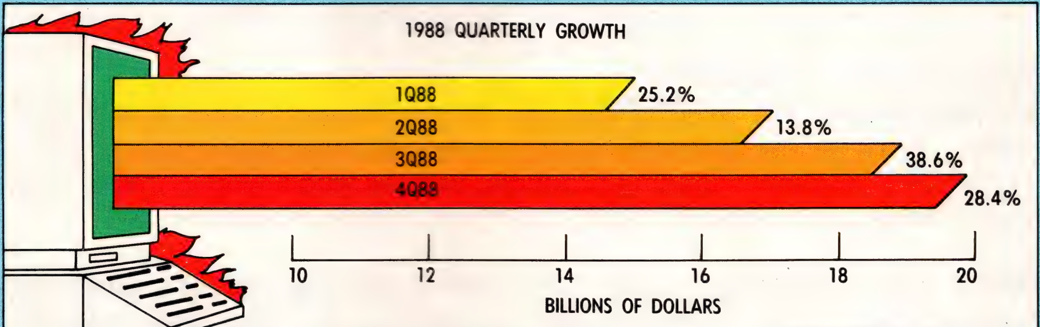
SOURCE: VLSI RESEARCH INC.

INDICATORS

The Market Place

A new analysis shows orders for computer equipment are stronger than expected; another puts chip sales at $72.7 billion in 1992.

U.S. COMPUTER SALES SIZZLE



SOURCE: KIDDER, PEABODY & CO. INC.

ESTIMATED WORLD SEMICONDUCTOR MARKET

(in billions of dollars)

	1987	1988	1989	1990	1991	1992
N. America	11.9	15.7	17.4	16.8	19.2	23.2
Japan	14.3	19.1	20.9	18.8	21.1	25.4
Europe	6.4	8.5	9.0	9.2	10.1	11.6
ROW	3.9	6.1	7.1	8.0	9.9	12.5
Total	36.5	49.4	54.4	52.8	60.3	72.7

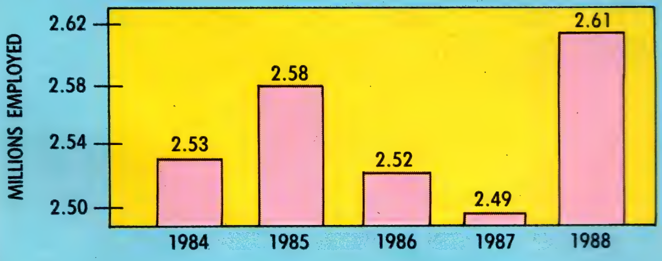
SOURCE: DATAQUEST INC.

The Work Place

U.S. EMPLOYMENT CONTINUES ITS UPSWING

	JUNE 1987	MAY 1988	JUNE 1988
COMPUTERS	430,800	452,900	459,700
COMSUMER PRODUCTS	60,600	60,400	61,100
COMMUNICATIONS SYSTEMS	605,400	598,500	600,200
SEMICONDCUTORS	245,500	261,500	265,700
COMPONENTS	377,500	394,200	399,200
SOFTWARE	241,000	274,400	280,400
ALL OTHER	529,200	548,100	543,700
TOTAL (in millions)	2.49	2.59	2.61

JUNE WORKFORCE: FOUR-YEAR TREND



SOURCE: AMERICAN ELECTRONICS ASSOCIATION

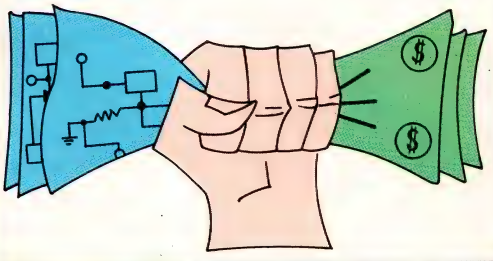
BASE PAY FOR U.S. ELECTRONIC DESIGNERS

Years of experience	1978	1987	1988
None	$16,400	$29,700	$30,700
Five	21,850	35,900	37,350
Ten	26,400	41,600	43,450
Twenty-five	31,200	50,550	52,300
By degree (with +10 years experience)			
B.S.	24,600	40,550	42,550
M.S.	27,200	43,000	46,500
Phd	30,850	51,750	NA*

Median salaries based poll of 12,791 engineers in 1988

* Insufficient response to survey

SOURCE: ENGINEERING MANPOWER COMMISSION,
AMERICAN ASSOCIATION OF ENGINEERING SOCIETIES



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PEOPLE TO WATCH

THE IEEE ELECTION IS UP FOR GRABS WITH NEW RULES AND FOUR CANDIDATES

'Approval' voting, aimed at blocking Feerst, is itself an issue

NEW YORK

When ballots go out to the 217,158 members of the Institute of Electrical and Electronics Engineers this month, voters will be faced with four choices for president and a new set of rules for choosing him. They will be able to cast their lot with any or even all of four candidates under the rules of approval-plurality voting, a relatively untested process the IEEE adopted last winter.

The rule change is an inspired attempt by the IEEE's board of directors to stop Irwin Feerst, a longtime IEEE critic. But ironically, it has become something of an election issue itself, particularly because of the surprise way the change was sprung on the membership. Equally ironic is the flavor of this year's campaign, which is concentrating heavily on the kinds of professional issues—pensions and fair treatment for engineers—that have been the hallmark of Feerst's 15-year battle with the IEEE hierarchy.

The four candidates are:

- Carleton Bayless, a Sacramento, Calif., consultant and one of two board nominees. He is a two-term board veteran and was executive vice president in 1977;
- Merrill W. Buckley Jr., the manager of program planning at GE/RCA Aerospace and Defense in Cherry Hill, N. J., also a two-term board veteran and the executive vice president in 1987. He broke from the ranks this year to run as a petition candidate;
- Eric Sumner, the second IEEE board nominee, and vice president of operations systems at AT&T Co.'s Bell Laboratories in Holmdel, N. J.. He has served one term on the IEEE board;
- and petition candidate Feerst, the Massapequa, N. Y., consultant and leader of the Committee of Concerned EEs, a splinter group that claims to support the interests of "the working engineer."

The IEEE changed the voting rules in December, in a move clearly aimed at narrowing Feerst's chances for victory this fall [*Electronics*, Dec. 17, 1987, p. 32]. Under the new system, voters can "approve" of as many candidates as they wish, and each vote counts equally. The candidate with the highest approval rating wins. The goal was to block Feerst from winning while the other nominees split the mainstream vote.

Running for IEEE president (clockwise from top left): AT&T's Sumner; communications consultant Bayless; GE/RCA Aerospace's Merrill W. Buckley Jr.; and consultant Irwin Feerst.

CLOSE CALL. Feerst came within a hair's-breadth of doing just that in 1986 when two board-nominated candidates split the mainstream vote. Current president Russell Drew won by just 242 votes out of 52,334 cast. Disheartened by the 1986 loss, Feerst waited until this year to wage his sixth guerilla campaign for the presidency of the IEEE. Now he's running again, promising as before to clean house at IEEE headquarters, to fire all permanent management, and to wage war against his avowed enemies—the executives and academics he says dominate the IEEE, and the foreign engineers he accuses of stealing American jobs. He also promises to lobby for taxes on imported high-tech products.

"The IEEE should represent the working engineer and not the executives and academics it represents now," Feerst says. "In the past few years, the IEEE has been led by a bunch of wimps. I'm not cut from that stuff."

Feerst's opponents variously characterize him as "crazy" and "brilliant," though they decry his ill-considered language (he indiscriminately uses the words "Nazi" and "fascist" to describe IEEE insiders). They also admit he has struck a chord with a growing constituency. "People vote for Irwin because they think the IEEE isn't doing enough in the areas for which he stands," says Buckley. "That means we have to spend more time with these issues."

So Buckley and Sumner are campaigning on professional issues that have been Feert's forte over the years. In the past, these might have gotten short shrift at the expense of less difficult subjects such as continuing education, a banner theme in virtually every IEEE election. "Our people are becoming increasingly concerned about pensions," says Buckley, who ran a petition campaign after the board failed to nominate him. "There are way too many people who end their careers with inadequate pensions because they've had to switch jobs or seek new employers several times in a career. The IEEE U. S. Activities Board [which has responsibility for the pension issue] should be more aggressive."

Sumner is more specific: "Defined benefit plans were OK in times of great stability, but when an engineer works for four companies in a lifetime, he ends up losing half his pension." The solution, he says, is a universal portable pension plan like those enjoyed by most college and university professors. He promises to launch a lobbying effort in Congress and to enlist the support of other engineering groups.

But not everyone is pushing pensions. Bayless, who retired from the Bell System in 1981 after 41 years at various parts of AT&T, has a campaign structured more like those of earlier IEEE presidential battles."Our members say maintaining our institute's technical excellence is our highest priority," he says. Where his opponents are tackling the Feerstian issues of inefficiency at IEEE headquarters and fair treatment for the engineer at the bench, Bayless discussed technical leadership and continuing education.

"[The] IEEE ought to be a member-service organization," says Bayless. "We've done some studies that show engineers are improperly utilized, that sometimes companies stockpile engineers as they're vying for defense contracts. Where there is a spotty oversupply of engineers in some places, we try to help."

Although Bayless says the sudden change in IEEE voting procedures was "responsible" and the new voting method is fair, he worries over whether voters will understand the system and take advantage of their multiple-vote capability. Buckley, for his part, reserves judgment on the plan, saying that "we'll have to give it our best support." But he adds that the IEEE "rushed into it too quickly and the members are suspicious."

Sumner is more negative: "The objective was to keep us from dividing the vote so that a rabble rouser could come in and claim victory," he says. "I prefer majority voting, and if elected I will certainly press for a constitutional amendment requiring majority elections."

SOLUTIONS. Recognizing that no matter who wins Feerst and his Committee of Concerned EEs will not disappear, the other three candidates all offer solutions for how to deal with a man who has been a thorn in the side of IEEE leadership for most of two decades. Bayless suggests IEEE's code of ethics could be used to quiet Feerst or remove him from the society, but warns, "We have to be careful not to make a martyr out of him."

Buckley hopes to lure Feerst's supporters to his camp. He says the IEEE must care for its members, and he's promising to elevate the issues of age discrimination, salary compression, and job stability to the top of the IEEE agenda if he wins.

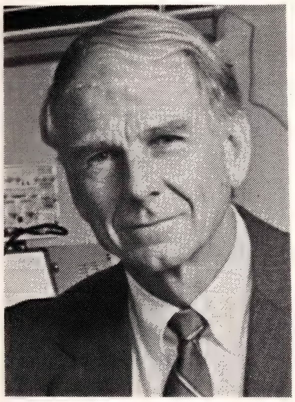
Sumner's push to rewrite the election rules again sums up his solution. "Once we have majority voting, then it's over. Let him speak. I like the Irwin Feersts of the world. I just don't want them to capture, by fluke, leading positions." *–Tobias Naegele*

SUPERCONDUCTIVITY IS DWIGHT'S NEXT CHALLENGE

SANTA BARBARA, CALIF.

Herbert P. Dwight is a pioneer—again. The 58-year-old executive, one of the first to see the commercial potential of laser technology in the early 1960s, is starting all over as chief executive officer of Superconductor Technologies Inc. As founder of Spectra-Physics Inc. in San Jose, Calif., Dwight led the laser company through its rough early years and eventually guided it to the top of its field when the technology finally matured.

Dwight's new challenge is in superconductivity. In August, he took over as the CEO of Superconductor Technologies, a high-flying startup with plenty of financial and technological muscle. The company's goal is not unusual—to be among the first to commercialize high-temperature superconductor technology—so the road ahead will be tough, crowded with a host of competitors that have also lined up with the very same objective in mind (see p. 105).


DWIGHT is leading technology toward the future again.

To that aim, Dwight brings his experience in shepherding the laser from laboratory phenomenon to mainstream technology. Recalling the early days at Spectra-Physics, Dwight says the challenge was actually similar to today's race to find commercial applications for superconductors. Back then, he says, "we could demonstrate [lasers] even though we didn't yet have the specific applications in hand." All they had, he recalls, was "a broad view of what lasers could be used for."

Dwight says the parallels between the technologies are clear. In the 1960s, lasers were tagged "a technology solution looking for an application," he recalls. But he says, "it never bothered us then, and it doesn't now." Superconductivity has been similarly named, but Dwight promises that as with the laser, "myriads of uses are out there, the most important of which can't be foreseen."

The steady growth of lasers into a substantial business over subsequent years rested on matching practical tasks with unfolding scientific advances, Dwight says. No one, for example, "could have predicted that lasers would be important in laying sewer pipe [as alignment instruments] or in nonimpact printers," he says. With superconductor technology, he adds, the same sort of surprises are likely. The future of Dwight's new company rests on its ability to exploit those opportunities as they arise. Dwight replaces Glen E. Penisten, another industry pioneer who is now a general partner in Alpha Partners, the Menlo Park, Calif., venture capital firm that cofounded Superconductor Technologies. Penisten searched for months before hand-picking Dwight as CEO.

Dwight's success at Spectra-Physics—he lifted the firm from the ground up into a $300 million company—was the standout factor in the decision. Spectra-Physics was acquired last year by Ciba-Geigy Corp., giving Dwight, its CEO since 1967 and former chairman of the American Electronics Association, time to pursue other things. He has been looking for the right challenge ever since.

So when Penisten offered him the top spot at Superconductor Technologies, Dwight couldn't resist. He relished the chance to run a company with the kind of standout technical talent Superconductor Technologies had already assembled—including J. Robert Schrieffer, who received the Nobel Prize for work on the theory of superconductivity. Other attractions included a solid financial footing with $8 million in capital, and a strong focus. The company is aiming its initial gaze at passive microwave devices and and interconnects for military infrared detection systems.

As in the laser business, the biggest worry for Superconductor Technologies is competition from abroad, especially Japan. Having already experienced the rigors of Japanese competition firsthand, Dwight observes that Japan's superconductivity initiative is well backed and "has to be feared." But the U.S., he says, has advantages stemming from individual companies and initiatives that can move more quickly than the centrally coordinated Japanese plan. So U. S. companies may be able to strike first and exploit promising niches sooner.

No dates are set for the first appearance of Superconductor Technologies' products, but "we have one to three years tattooed on our heads," he says. As in the laser industry, those companies that can dig a toehold in superconductivity early in the game will have ample opportunity "to grow into very significant enterprises." This is what Dwight aims to do—again. *–Larry Waller*

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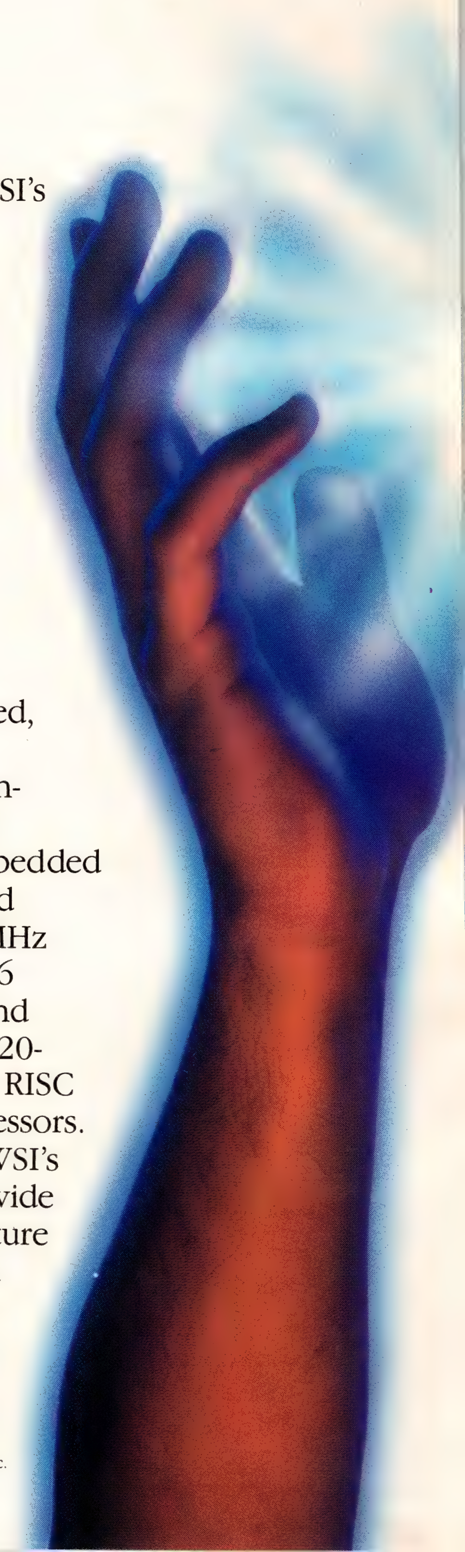

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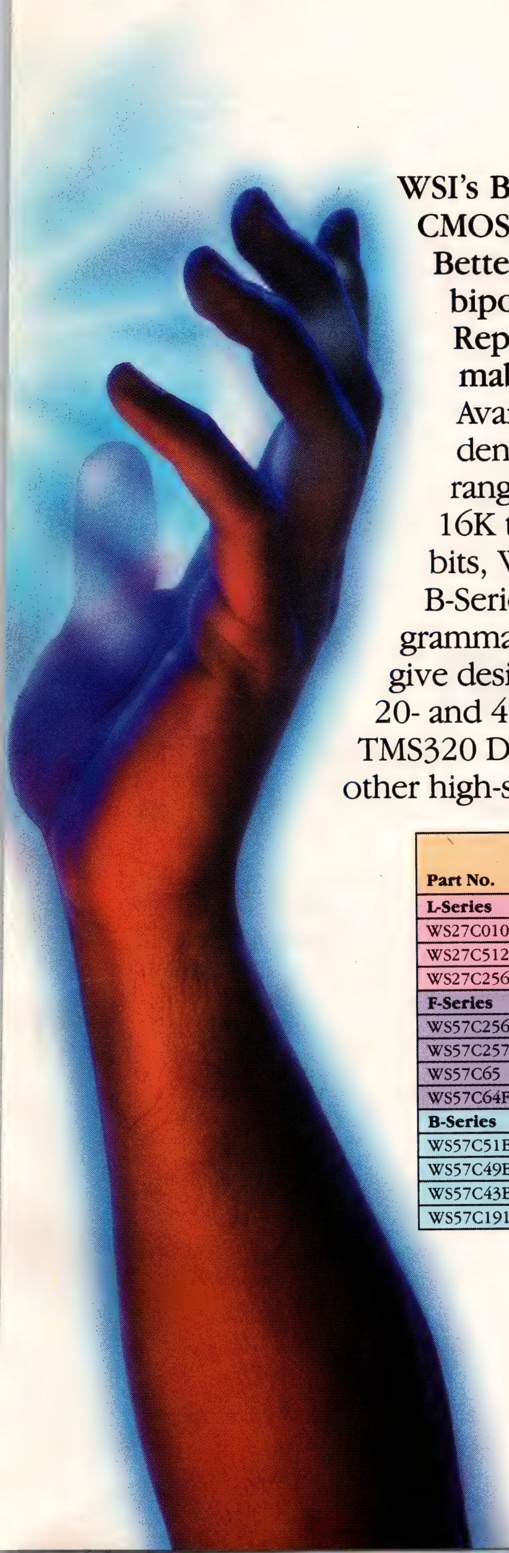

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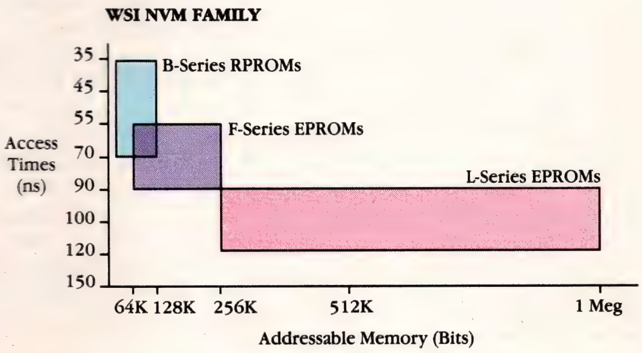

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READER'S REPORT

The problem lies in patents

To the editor: While people instinctively side with George Gilder (who champions individuals), the power lies with Charles Ferguson (who champions large corporations) [*Electronics,* July 1988, p. 3].

Imagine a world in which U.S. patents are 99.9% valid. The inventive forces of U. S. engineers would be unleashed and the corporate monopolies in patents and their profits would end. No longer would corporate size and political leverage determine who profits. Profits would go to inventors and those licensed to produce their inventions.

In the past, ineffective patent right protection has shackled America's inventive resources. Since World War II, foreign corporations have effectively displaced domestic firms in worldwide markets because U. S. technology is free for the taking. Corporations don't fear patent infringement since patents are easy invalidated by courts. Foreign corporations, like their American counterparts, are engaging in this judicial slaughtering of U. S. patents.

The domestic corporations' answer to the loss of markets is government intervention, heavy research and development subsidies, tax breaks, and import controls. However, the loss of markets has increased with increased subsidies. American engineers can look forward to changing employers as domestic corporations continue to sell out to foreign firms.

Ultimately, I see Congress and the courts taking their marching orders from foreign corporations.

We are witnessing a transfer of global power. While I sympathize with George Gilder's view, I feel Charles Ferguson's will prevail in the end.

James Constant
Claremont, Calif.

"The Springs" is not Camelot

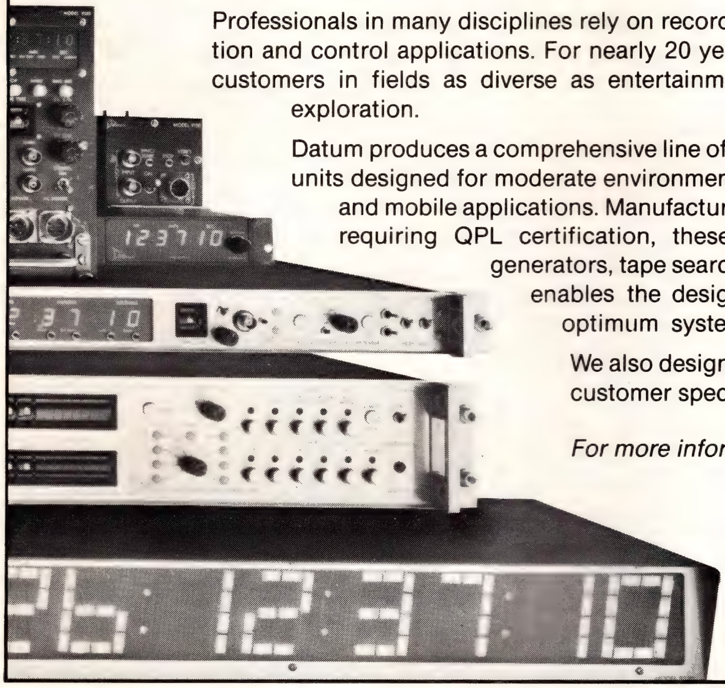
To the editor: I have to respond to your "Letter from Colorado Springs." It is the same line that has been dished out by the Chamber of Commerce for years. It brings in people from all over, looking for work. But the truth about the Springs is quite different.

Openings have been, and continue to be, scarce. Because they can't find work, PhDs and mechanical engineers deliver pizza. Most technician's job openings are through temporary employment agencies, which pay $6 an hour and have no benefits. Persons coming from highly unionized states will discover that employees have almost no rights in Colorado. They can be discharged without cause for any reason, at any time.

Because the average age is so low in the Springs, walking into a shopping mall is likely to remind a baby boomer of a scene from *Logan's Run.* If you are a successful Republican, you'll love it. Furthermore, because the inhabitants are all so young, they are very self-centered and indifferent to those who haven't done well. As you talk to people about others who've been put out of their jobs unfairly and without notice, they come back with a story of their own and act as if it is just the way it is.

And so it is in Colorado Springs. If you are a manufacturer, there are thousands of gullible young people eager to be walked all over. If you are an employee, don't go there without a job. If you are offered a job there, get an ironclad contract in writing, because if your employer does you dirt, nobody will give a damn and you will have *no* legal recourse.

Michael Larkin
Salem, Ore.



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BUILDING NEW SOFTWARE FROM REUSABLE BLOCKS

A technique for better quality and faster development

It's taken a long time, but software engineering is finally acclimating itself to the world of mass-production. Long considered more of an art than a science, software design is now undergoing the same evolutionary change that helped take the wizardry out of chip design.

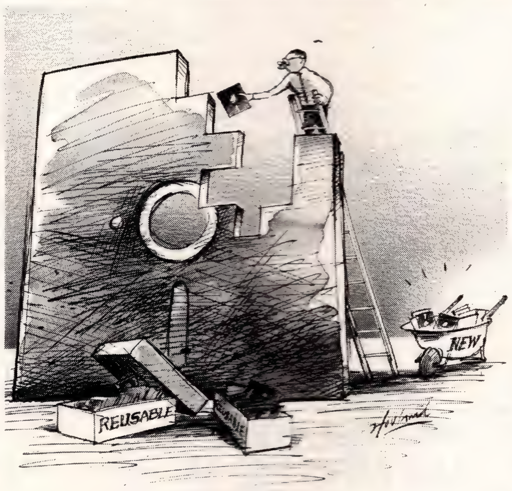
By emphasizing reusable building blocks and generic shells that can be fine-tuned for specific applications, both systems and software companies are trying to do for software what fast-turnaround application-specific integrated circuits—standard cells, gate arrays, and programmable logic arrays—have done for the chip business. They're seeking dramatic improvements in productivity, quality, and speed to market their software products.

The proliferation of vast computer systems in business—from airlines' on-line transaction-processing systems to banks' automatic teller networks—"cries for speeding up the ponderous software systems design process, which has improved at only about 5% per year," says Eric Sumner, vice president for operations systems at AT&T Co.'s Bell Laboratories in Holmdel, N. J. While hardware processing power is doubling every 18 months or so, software is improving at a much slower, indeterminate rate.

The problem is that designing software is roughly two to four times more difficult than designing hardware, Sumner says. While a circuit designer might be able to produce a simple chip design in one week, and a board designer could conceivably polish off an analogous printed-circuit board design in two weeks, Sumner suggests it would take at least a month for a software engineer to complete a project of similar complexity.

Three years ago, AT&T launched a software productivity program with ambitious goals: a 300% increase in productivity by 1991 and a 10-times reduction in software defects, or bugs, by 1992. So now, with a focus on reusable software modules, coupled with emphasis on advanced languages, such as C++, and tools, such as those provided by a range of CASE companies—vendors of computer-aided software engineering tools—AT&T is beginning to meet its goals.

The key, Sumner says, is creating software that not only does the job in a given application, but can also be reused as a "component" of some future system. The idea stems from the techniques used in application-specific integrated circuit design, in which predefined standard cells are stored in a data base and can be called into a design when the engineer specifies the function that he needs—an adder or a flip-flop, for example.



By creating a library of functionally defined software components that can be pieced together in similar fashion, Bell Labs and others aim to drastically cut the time and cost of new-product development. "Reusable software building blocks can give you better quality, a unified user interface across a multiproduct line, and better speed to market," says Yogen Dalal, vice president for product development at Claris Corp. in Mountain View, Calif. Adds AT&T's Sumner: "Customers don't care how many lines of code there are, they just want fewer defects per system. And reused code is invariably better quality than new code because it has already been proven in the field."

IBM Corp. originated the idea of reuse in the 1960s when it introduced the concept of the operating system—general software that would take care of the common functions shared across many applications, says Richard B. Butler, director for systems programming at IBM's Data Systems Division in Poughkeepsie, N. Y. "You need to define reuse at a broader level than just modules and blocks," he says. "You can start at reusing systems—the idea of evolution rather than revolution in new systems design."

The desire to reuse software is one factor behind IBM's Systems Application Architecture program interface standard. SAA, when ready, will permit the same application to run in four environments—OS/2, AS 400, MVS, and VM. "SAA isn't going to give you the identical application for every level, but it will be close," Butler says. The result is that IBM will be able to provide applications, compatibility, and connectivity across its product line with relatively little effort. "Wherever you standardize, you can focus on the job you're doing," Butler explains. "And you can do the job better than if you were doing it four times over in four different ways." In the Unix world, the Common Application Environment developed by X/Open Ltd. of San Francisco has similar goals.

As attractive as the modular approach is, however, traps abound for the unwary engineer. AT&T's Sumner admits that "it takes a little more effort to build a reusable module than to build a straight-away program." That's something companies need to deal with, says IBM's Butler, because the productivity of a software engineer is traditionally measured in terms of the lines of code he produces. "You need to give credit to the programmer who takes the time to make his piece of software reusable," he says. "But at the same time, you don't want to penalize the person who uses reusable blocks." The answer, he concludes, may be to credit both: the engineer whose code is reused 10 times gets credit for having written 10-times the number of lines in the module, while the designer who reuses that code is given credit for those lines as if he started from scratch.

Modular software also presents other potential pitfalls. As with ASIC hardware, users must be willing to pay a significant performance penalty. But Sumner says the potential savings are

by Tobias Naegele

worth the price because hardware performance is advancing so rapidly. "The one thing we're willing to sacrifice is performance," he says. "We'll throw away 20% of our computer power in order to reuse software."

And even the process of making software reusable is tough. There is a very fine line in determining how large or small the software modules should be, says Howard L. Yudkin, president and chief executive officer of the Software Productivity Consortium in Reston, Va. "If the reusable modules are too small, the work saved is minimal," he says. "If parts are too big, they become too specialized. We must build from parts of reasonable size to eliminate rework."

A joint venture of 13 leading aerospace and defense contractors, including Boeing, McDonnell Douglas, Harris, and Ford Aerospace, the Software Productivity Consortium is working around that balance, with a two-tiered approach. "There are some cases—math, transaction processing, user interfaces—that have wide application and can be defined to amortize very well," Yudkin says. But in other cases, such as defining a feedback control, that approach won't work. Instead, his group is looking at building reusable generic shells that, given well-defined rules and methodologies, can be modified for the task at hand.

AT&T is building its library by demanding that every software program return a minimum of 10% of its new end-product code to the library shelves. But that alone is not enough, says Dalal of Claris. "You not only have to legislate reuse through policy, but you have to create an environment where people are excited to use each other's software as well," he says.

AT&T seems to have succeeded on that score too. Reuse at AT&T averaged 22% by late 1987, and Sumner says progress since has the company on track to meet its goal of 33% late this year. In one recent project that included 1.2 million lines of software code, 87% was reused.

"We would like to go to 90% reuse," Sumner says. "I have no doubt that 10 to 15 years from now we'll be at 90% on average. Software reuse is our sustainable advantage." How does that transfer into increased productivity? Sumner says that in 1986, the standard rate of software production was 5,000 lines of code per staff year. Two recent network operations systems projects, both started from scratch, averaged 15,000 lines of code per staff year, thanks in part to reuse rates of 66% and 70%.

But reuse is not the only answer. "The first place we try to maximize productivity is in hiring," says Geoffrey J. Bunza, director of engineering in the Design Analysis Division of Mentor Graphics Corp. of Beaverton, Ore. "We've found that one very good software engineer is worth two, maybe three, ordinary ones." Also important, he says, is keeping his engineers challenged and motivated. While most software engineering environments—including those at Bell Labs—lean toward having two or three engineers sharing a space, Bunza says, "we give our engineers an office with a door."

Mentor also has an automated reporting system that analyzes errors and performance on each ongoing software project, Bunza says. Measuring a variety of factors, the system produces a composite view of bugs and an analysis of the severity of problems and enhancements the project is experiencing. This is meshed with a set of target dates for specific milestones to produce a final weekly report. "The technique has enabled us to learn whether or not the product is mature enough for market," Bunza says.

Ultimately, however, managing software is "a little like managing innovation," Bunza explains. "You can't just go out and say, 'this week, we're going to make a breakthrough.' You can't just tell your engineers that they've got to increase productivity by 50% a month. You've got to give them the right environment, the right tools, the right challenge, or it won't work."

HOW THE 'WHAT-IF' LAB HELPS DEC AND HP HELP THEIR CUSTOMERS

Computer manufacturers need more than sales offices and demonstration centers to showcase the full breadth of solutions they can provide for customers. Two of the big names in the business, Digital Equipment Corp. and Hewlett-Packard Co., have found that out. So DEC has set up a worldwide chain of centers to act as problem-solving labs for customers and HP is in the process of doing so.

DEC now has 39 Application Technology Centers that link the latest DEC hardware, software, and services into a networked resource. They provide enough return on investment to please DEC management, so 12 more are planned, says Laura Chester, ACT program manager in Stow, Mass. She says customers can bring in their problems and have expert consultants work out a solution. The centers offer specialized help: the Detroit ACT, for example, is attuned to the needs of the automotive industry.

At HP, Walter Skowron calls the company's Fort Collins, Colo., Technical Systems Sector's demonstration center "HP's what-if laboratory." It's a place where customers can check out various approaches to their tasks. Skowron is the demonstration center manager for the Fort Collins site and for a portion of one that opens this month in Cupertino, Calif.

He says the two are the forerunners for several other sites, including Böblingen, West Germany, and Hong Kong—existing demonstration sites that will be upgraded to include a broader range of equipment.

Customers can come to Fort Collins and Cupertino now to determine how their applications would run on HP systems ranging from personal computers to minicomputers. The company has long maintained demonstration centers but is broadening the concept to integrate manufacturing and office automation with its full breadth of systems.

Fort Collins is heavily oriented toward computer-aided design and manufacturing because it's sponsored by the company's Technical Systems Sector. But the site can also bring into play the office automation expertise of the Business Systems Sector. "The kinds of things we can do would be very difficult to do simply by using sales people in a sales office," Skowron says.

At DEC, Chester says the company learned the same thing from its experience in the three kinds of regional centers from which the ACT concept evolved: office solution, field application, and CAD/CAM centers. She says ACTs combine the best of the three and increase functionality with networking and locally available consultants.

While the centers improve service, both cost and return are substantial. Chester says DEC has invested "many millions of dollars" in each center to equip, staff, and operate it. A typical center includes four large VAX systems and a broad complement of work stations, terminals, and peripherals.

A sophisticated tracking system tabulates the number of customers and the amount of business the site generates. Chester says DEC measures the revenues traceable to the centers in "multimillions of dollars; the corporation is very pleased."

And, apparently, so are the customers. A major airline, for example, estimates that an ACT-derived computerized solution to periodic aircraft engine maintenance, which has always been done manually, cut overhaul costs by 50% at its San Francisco International Airport maintenance center. The solution was worked out at an ACT in Santa Clara, Calif., as well as at DEC's Enfield, Conn., manufacturing center.

–Lawrence Curran

BOOK REVIEW

HERE'S A PRIMER ON VENTURE CAPITAL

THE ARTHUR YOUNG GUIDE TO RAISING VENTURE CAPITAL
by G. Steven Burrill and Craig T. Norback
Blue Ridge Summit, Pa.: Liberty House, $24.95

The publishers of the new *Arthur Young Guide to Raising Venture Capital* should have skipped the hardcover edition and gone directly for the $4.95 paperback market. Its format of giving each of a great many topics a few pithy paragraphs is better suited to a paperback outline series. It's also great for budding entrepreneurs who like to stuff research materials into the back pocket of their blue jeans. But with just 135 pages of text and 117 pages of appendices and lists, The Arthur Young guide can hardly be considered a definitive work.

Nevertheless, it is worth the read for the uninitiated. Readers are provided with some useful insights into the mentality of venture capitalists. For example, venture capitalists are chiefly interested in funding clients between the ages of 25 and 35, when motivation, energy, and the willingness to take risks are at their peak.

Would-be entrepreneurs over 40 can take some solace in the fact that a wonder kid is nothing without a seasoned management team. Having technology veterans with a good track record is more important than a good idea in bringing a product success. "Teams win; superstars lose" is the seminal line the authors use to drive this point home. In fact, the dicotomy between the engineer/entrepreneur and the manager/profit maker seems to be the key to appreciating the venture capitalist's perspective. For example, although everybody would like to make money, the true manager is as intrigued with the discipline of making money as the engineer is intrigued with the discipline of circuit design.

Because the bottom line is that the entrepreneur needs help, the authors spend a good deal of time outlining the requirements of a business plan and the structuring of the deal. Unfortunately, the book should remind readers of this variation on the cynic's description of a real estate rental contract: a list of the venture capitalist's (landlord's) rights and the entrepreneur's (renter's) responsibilities.

The authors—Burrill, a partner at Arthur Young, and Norback, a consultant—point out a cold, hard, and obvious fact to budding entrepreneurs: they cannot expect to keep control of their fledgling companies once financing comes from outside. For one thing, voting rights reflect investment commitments, and he who has the gold makes the rules. But over and above that, they say, successive rounds of financing—particularly going public with a common stock offering—dilute the inventor's voting block down to 10% or 15% by the fourth refinancing.

Another eye-opener is the book's chapter, Due Diligence, which is financial jargon for investigating the entrepreneur's background. The chapter amplifies the book's oft-repeated theme that people are more important than ideas and products. All in all, the book adds up to light reading on a heavy topic, which isn't a bad way for neophytes to introduce themselves to the subject. —*Jack Shandle*

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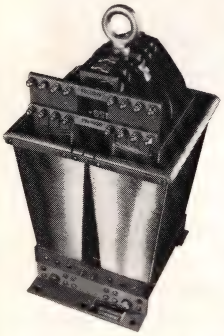

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MEETINGS

A select group of 1,000 to 1,500 attendees will take a fresh look at clean rooms, stress-test chambers, and other artificial environments at the Ninth International Symposium on Contamination Control, which will be held in Los Angeles Sept. 26-30.

Six tutorial sessions will be available for people just getting involved in creating or managing such environments, but the seminar itself will focus on the technology's future. Keynote speaker Joel A. Barker will explore technology development over the next two decades with emphasis on new business opportunities. Barker, president of Infinity Ltd., St. Paul, Minn., is a consultant specializing in the strategic exploration of new technologies.

The symposium will be held in the Century Plaza Hotel. For more information, contact the Institute of Environmental Sciences, 940 E. Northwest Highway, Mt. Prospect, Ill. 60056; (312) 255-1561.

In October, the IEEE International Conference on Computer Design will delve into the interactions between system design, logic circuit analysis, memory design, testing, and other disciplines. Among the speakers will be Dr. H. Kung of Carnegie Mellon University, whose topic will be "When will the widespread use of parallel computers become a reality?"

The conference will be held Oct. 3-5 at the Rye Town Hilton Hotel, Rye Brook, N.Y. The person to contact is Glenda McBride, IEEE Computer Society, 1730 Massachusetts Ave., N. W., Washington, D. C. 20036; (202) 371-1013.

Other conventions, shows and expositions on the *Electronics* calendar include:

International Congress on Transportation Electronics, Oct. 17-18 at the Hyatt Regency Hotel, Dearborn, Mich. Contact Louis Nagy, Electrical and Electronics Engineering Dept., General Motors Research Laboratories, Warren, Mich. 48090; (313) 986-1636.

Seventh International Congress on Applications of Lasers & Electro-Optics (ICALEO '88), Oct. 30-Nov. 4 at the Santa Clara Convention Center, Santa Clara, Calif. Contact Larry Lotridge, OPTCON '88, 1816 Jefferson Pl., N.W., Washington, D.C. 20036; (202) 223-8130.

Federal Computer Conference and Defense and Government Computer-Graphics Conference, Oct. 26-28, a joint conference is being held in the Washington Convention Center, Washington, D. C. Contact the National Council for Education and Information Strategies, 15200 Shady Grove Rd. #350, Rockville, Md. 20850; (301) 676-2818.

Autofact, Oct. 31-Nov. 2 at McCormick Place East, Chicago. Contact Jill Vanderlin, Society of Manufacturing Engineers, One SME Dr., P. O. Box 930, Dearborn, Mich. 48121; (313) 271-0023.

The Unix Operating System Exposition and Conference, Oct. 31-Nov. 2 at the Javits Center, New York, N. Y. Contact National Expositions Inc., 15 W. 39th St., New York, N. Y. 10018; (212) 391-9111.

1988 Gallium Arsenide REL Workshop, Nov. 6 at the Opryland Hotel, Nashville, Tenn. Contact William Roesch, TriQuint Semiconductor; (503) 644-3535, ext. 4143.

IEEE International Conference on Computer Aided Design (ICCAD), Nov. 7-10. The contact person is Al Jimenez, Pro CASE, 3130 Dela Cruz Blvd., Suite 100, Santa Clara, Calif. 95054; (408) 727-0714.

Supercomputing '88, Nov. 14-18 at the Hyatt Orlando, Kissimmee, Fla. The contact is George Michael, Lawrence Livermore Labs, P. O. Box 808, Livermore, Calif. 94550; (415) 422-4239.

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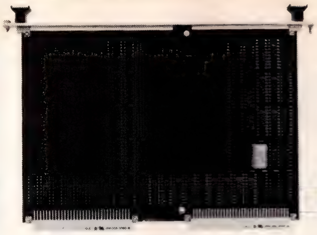

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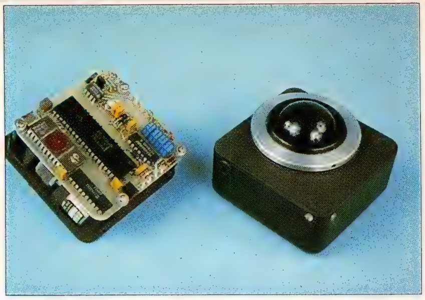

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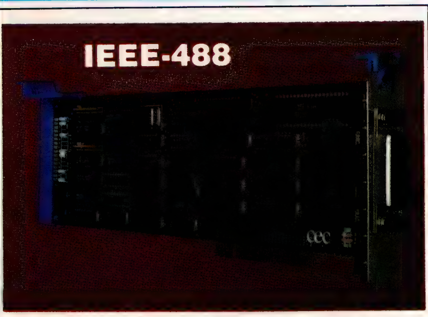

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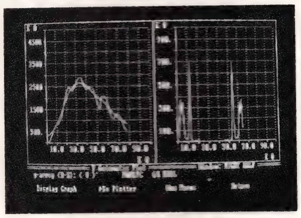

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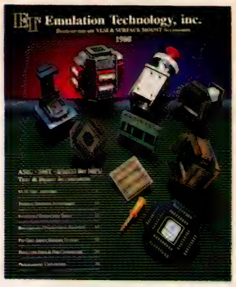

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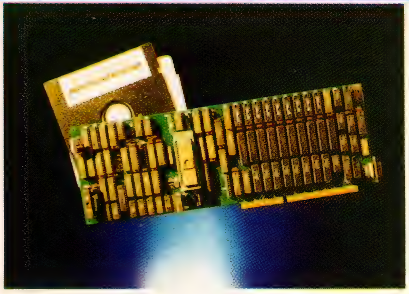

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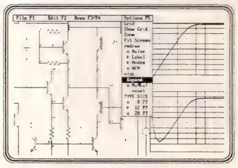

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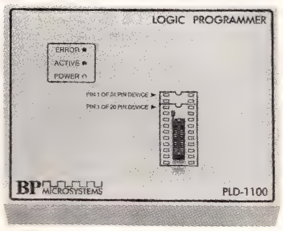

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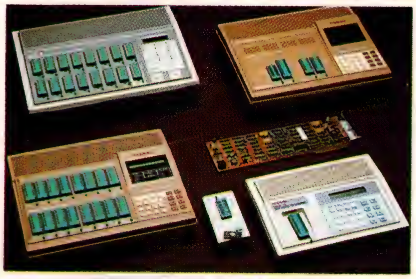

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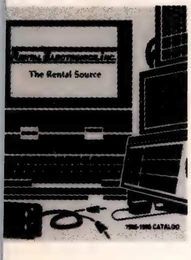

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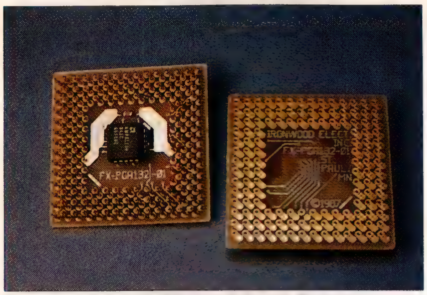

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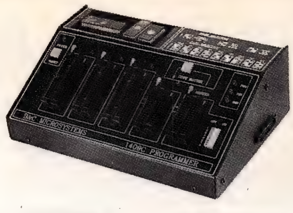

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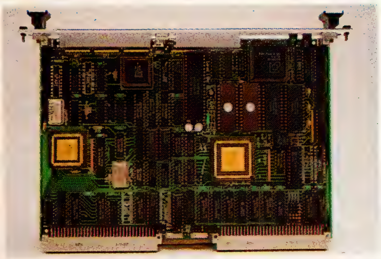

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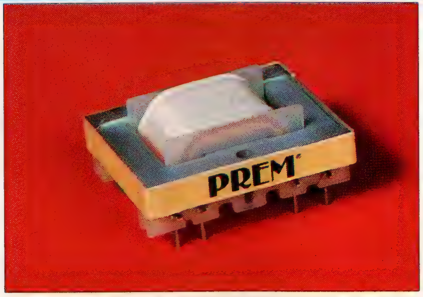

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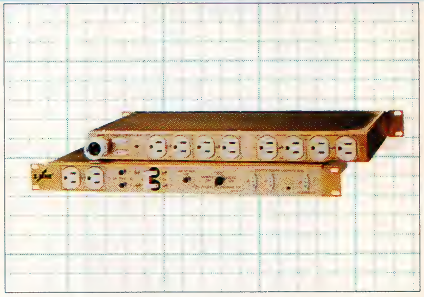

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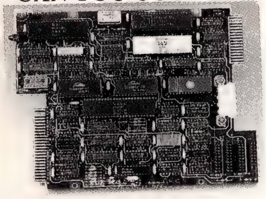

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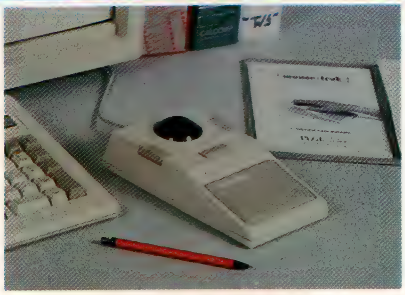

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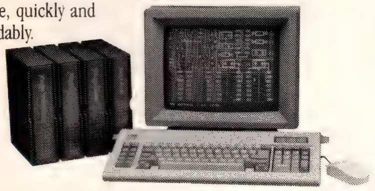

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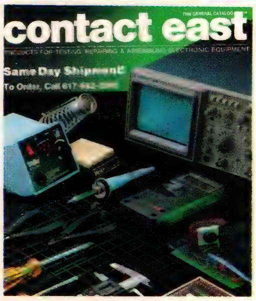

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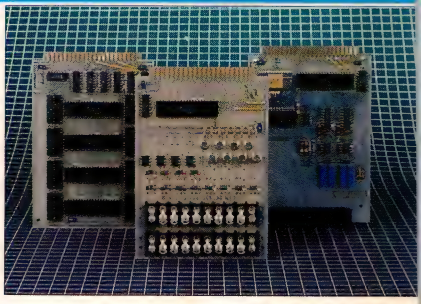

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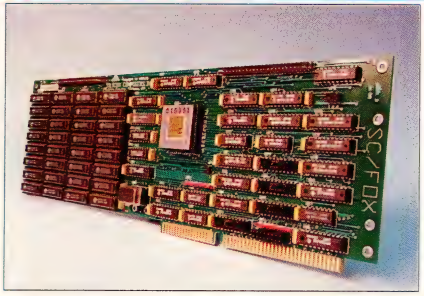

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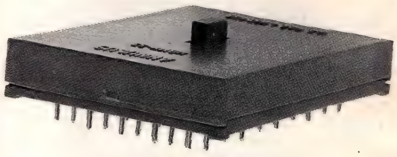

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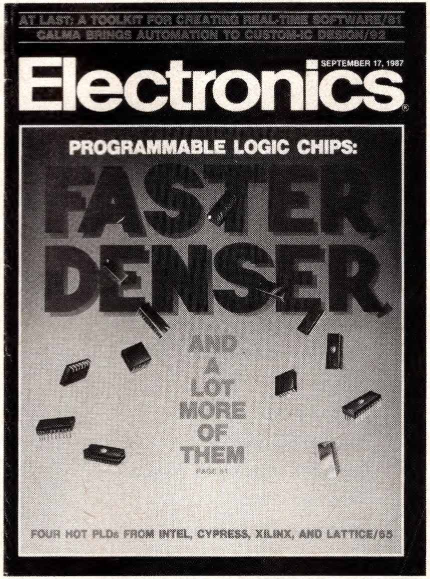
UPDATE: EPLD MAKERS HEAR CASH REGISTERS RING

The word to describe four of the prime players in the hot market for erasable programmable logic devices is "happy." Orders for parts have been pouring in to Cypress, Intel, Lattice, and Xilinx ever since the companies launched major EPLD lines [*Electronics*, Sept. 17, 1987, p. 67].

At Cypress Semiconductor Corp. in San Jose, Calif., executives are so pleased with the reception their first three application-specific EPLDs got that they plan to expand the family. Meanwhile, two of the three chips announced a year ago are going great guns and the third is about to bow. The three, 28-pin EPLDs are designated CY7C330, CY7C331, and CY7C332. They have clock rates of 33 to 50 MHz, are ultraviolet erasable, and are different from traditional general-purpose programmable logic devices because each member fills different system needs: the 330 is for synchronous state machine applications; the 331 is for those requiring asynchronous registered PLDs; and the 332 is for registered combinatorial applications.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PROGRAMMABLE LOGIC CHIPS:
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PAGE 81
FOUR HOT PLDs FROM INTEL, CYPRESS, XILINX, AND LATTICE/65

Orders and queries are pouring in at Cypress, Intel, Lattice, and Xilinx

"Two things surprised us, pleasantly," says Dane Elliot, manager of applications engineering. "One was the overwhelming response to the parts and the other was the performance." The 330 was first available in sample quantities last October. Then came the 331 in January. Since then, he says, "we have shipped literally thousands of samples to hundreds of companies." There are already a number of major design wins for both. Moreover, though the company expected a 50-50 yield on 33- and 50-MHz parts, almost all of the good dice have yielded 50-MHz devices.

The one glitch was with the CY7C332, a registered combinatorial part that eliminated the external register often needed with such a device. It has 12 input/output macrocells, 13 input macrocells, a single clock with two inputs, 192 product terms, and a separate pin for synchronous, rather than asynchronous, loading of data. "Customers wanted more," Elliot says. "Mainly they wanted two independent clocks instead of one clock with two inputs. This allows the register to be configured as a true combinatorial register, a D-type flip-flop." So Cypress redesigned the chip; samples are due in October.

Also in the works are 60- to 75-MHz versions as well as a fourth one, scheduled for introduction in mid-1989. Designated the CY7C333, it is a more generic part with added flexibility. "We have more than enough room," Elliot says, "even with a 10% or 20% speed penalty we would still beat everything else in the industry."

Similarly satisfied is Intel Corp.'s Lawrence Palley, PLD product marketing manager in Folsom, Calif. The company's first proprietary PLD, the 25-ns 5AC312, has chalked up "hundreds of design wins," he says. Designed to address the system I/O problems encountered in high-performance microprocessor-based systems, it is now entering full production. The key to its success is its ability to address the performance needs of 80286- and 80386-based systems while latching and holding incoming data at various points in the system.

Intel is completing development of a performance-enhanced version of the 312—with samples to be ready at year's end—as well as on a third specialized EPLD designed to resolve microprocessor-to-memory-bus throughput problems. Samples are scheduled to be delivered in the first quarter of next year.

Up north in Beaverton, Ore., Lattice Semiconductor Corp. reports almost 1,000 inquiries since it began shipping samples of its groundbreaking electrically erasable PLD, renamed GAL6001, late last year. The design combines flexibility of the programmable-AND/programmable-OR structure of a programmable logic array and such PLA-type features as macrocells and buried registers. With volume production scheduled to start this month, the only real problem with the device, says Rod Strange, director of applications engineering, was the original name, 39V18. "Because we began with a generic programmable array logic architecture in the GAL16V8 and GAL20V10, people assumed it was the same type of device and tried using it that way."

However, a PLA-type device is more flexible, with 38 inputs driving the programmable AND array—each of which has an associated macrocell, 10 of which are intended for I/O, 10 for input, 10 for output and eight buried state logic cells. The programmable OR array has 64 product terms; each is a function of the entire AND array.

Finally, in San Jose, officials at Xilinx Inc. say they have been inundated with orders since the introduction of the first parts in the company's second-generation 1,800-to-9,000-gate XL3000 series of programmable gate arrays with random-access-memory-based logic cells. Wes Patterson, executive vice president, says since the company began shipping its 1,800-gate XL3020 and 9,000-gate 3090 samples, it's been selling more per quarter than it sold in the first two years of its first-generation devices.

With these first two parts in production, the company is filling in the gaps. It just achieved first silicon on the 4,200-gate XL3042 and the 3,000-gate XL3030 and expects samples in October. Design on a fourth part, the 6,400-gate XL3064, is complete, and the company is pushing to launch it before year's end. *–Bernard Cole*

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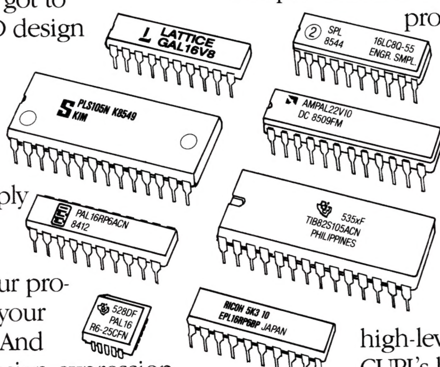

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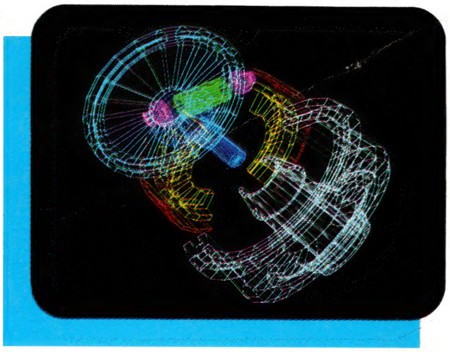

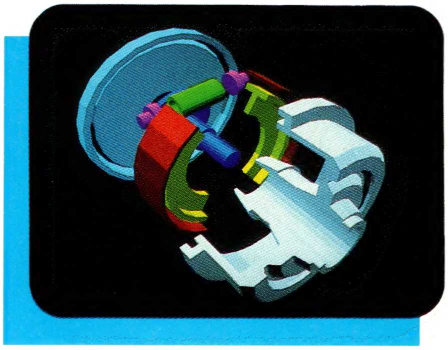

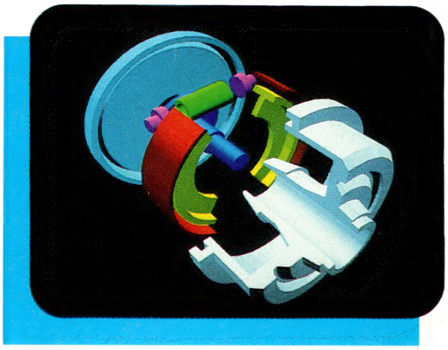

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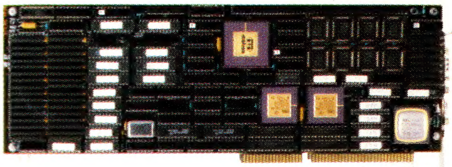

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